TGA2760-SM

10 – 11.7 GHz Power Amplifier

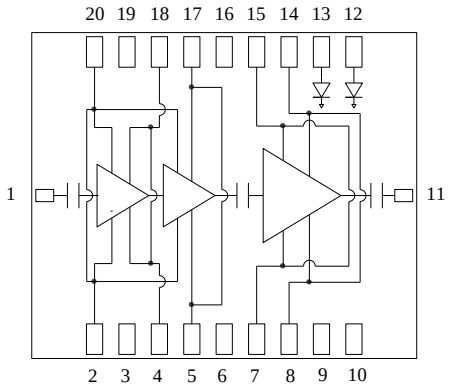
Product Overview

Qorvo's TGA2760-SM is a packaged X-band high power amplifier utilizing Qorvo's production GaAs pHEMT and GaN processes. The TGA2760-SM operates from 10 – 11.7GHz and typically provides 16W saturated power with power-added efficiency of 36% and large signal gain 30dB. Third-order intermodulation is better than -30dBc at 3dB backed off from Psat. Along with the higher performance, an additional feature is an integrated power detector allowing the user to accurately monitor the output power of the unit.

The TGA2760-SM is packaged in a small air-cavity surface mount package and matched to 50 ohms with integrated DC blocking capacitors on both RF I/O ports simplifying system integration.

Lead-free and RoHS compliant.

Functional Block Diagram



Top View

20-Lead 8.0 x 10.0 x 2 mm Package

Key Features

- Frequency Range: 10 – 11.7 GHz
- Power: +42 dBm Psat
- Gain: 33 dB
- Integrated Power Detector
- Bias: $V_{D1} = V_{D2} = +7$ V, $I_{D1} + I_{D2} = 1000$ mA, $V_{D3} = +28$ V, $I_{D3} = 260$ mA
- Package Dimensions: 8.0 x 10.0 x 2 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details

Applications

- Point-to-Point Radio

Ordering Information

Part No.	Description
TGA2760-SM-T/R	500 pieces on a 7" reel (standard)
TGA2760-SM, Sample	Waffle Tray with 2 pcs
TGA2760-SM, Eval Board	Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Drain Voltage, V_{D1}, V_{D2}	+9 V
Drain Voltage, V_{D3}	+32 V
Drain Current, I_{D1} + I_{D2}	3850 mA
Drain Current, I_{D3}	2000 mA
Power Dissipation, Driver Stages, P_{DISS}	14.8 W
Power Dissipation, Final Stage, P_{DISS}	28.8 W
RF Input Power, CW, 50 Ω, T = 25 °C	+29 dBm
Mounting Temperature (30 Seconds)	260 °C
Storage Temperature	−40 to 150 °C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Operating Temp. Range	−40	+25	+85	°C
V_{D1}, V_{D2}		+7		V
V_{D3}		+28		V
I_{D1} + I_{D2}		1000		mA
I_{D3}		260		mA
V_{G12}		−0.7		V
V_{G3}		−2.6		V
I_{D1} + I_{D2} drive (at +39 dBm Pout)		1018		mA
I_{D3} drive (at +39 dBm Pout)		930		mA

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

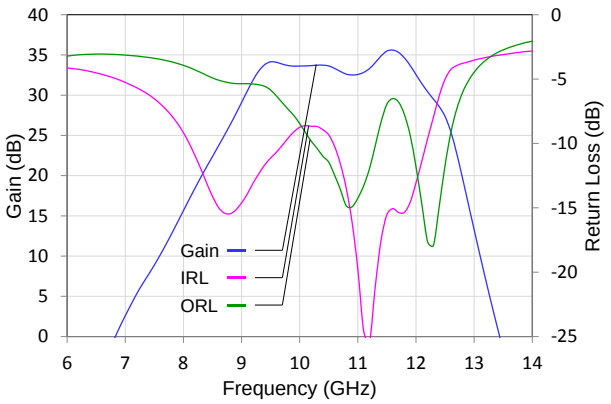
Parameter	Conditions (1)	Min	Typ	Max	Units
RF Frequency Range		10		11.7	GHz
Small Signal Gain		27	33		dB
Input Return Loss, IRL			8		dB
Output Return Loss, ORL			8		dB
Output Power at Pin = +12 dBm		+39.5	+42		dBm
Power Added Efficiency			36		%
Output Third Order Intercept, TOI @ 30 dBm/Tone			+52		dBm
Gain Temperature Coefficient			−0.05		dB / °C
Power Temperature Coefficient			−0.01		dBm / °C

Notes:
1. Test conditions unless otherwise noted: $V_{D1} = V_{D2} = +7$ V, $I_{D1} + I_{D2} = 1000$ mA, $V_{G1} = V_{G2} = -0.7$ V, $V_{D3-} = +28$ V, $I_{D3} = 260$ mA, $V_{G3} = -2.6$ V, Temp = +25 °C, $Z_0 = 50$ Ω

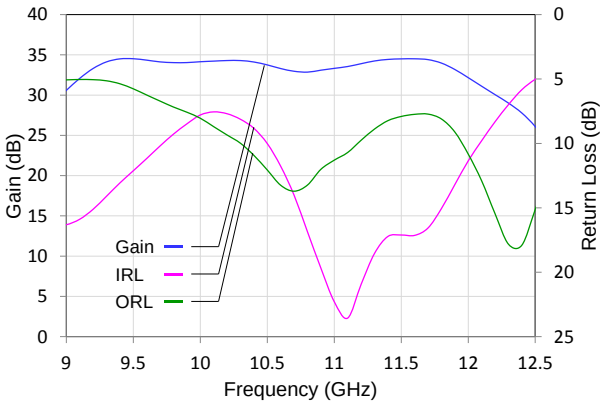
Performance Plots

Test conditions unless otherwise noted: $V_{D1} = V_{D2} = +7$ V, $I_{D1} + I_{D2} = 1000$ mA, $V_{G1} = V_{G2} = -0.7$ V, $V_{D3} = +28$ V, $I_{D3} = 260$ mA, $V_{G3} = -2.6$ V, Temp = +25 °C, $Z_0 = 50\ \Omega$

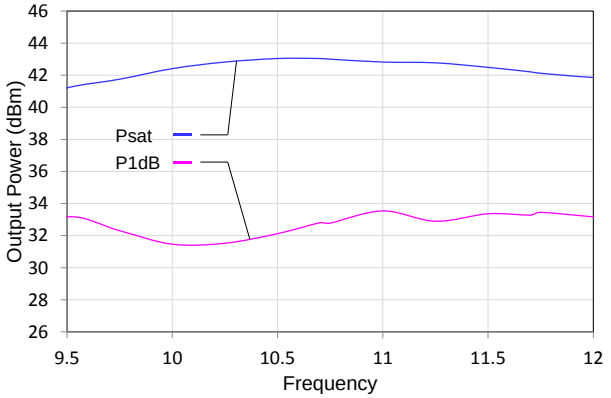
S-Parameter vs. Frequency



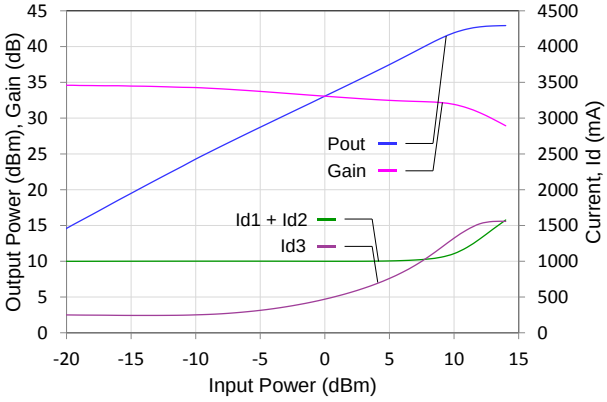
S-Parameter vs. Frequency



Output Power vs. Frequency

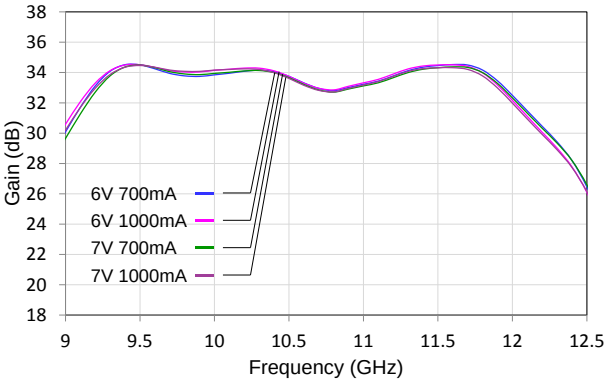


Pout, Gain, Id vs. Pin @ 10.5 GHz



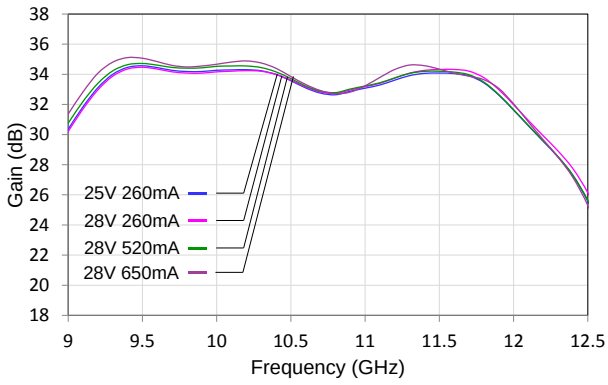
Gain vs. Frequency vs. Bias (Vd1 and Vd2)

Vd3 = 28 V, Id3 = 260 mA, Vg3 = -2.6 V Typical



Gain vs. Frequency vs. Bias (Vd3)

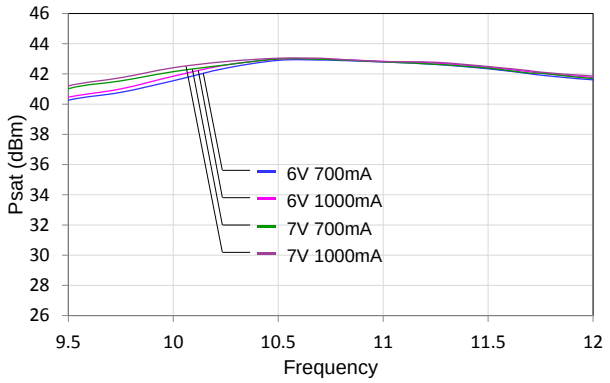
Vd1 = Vd2 = 7 V, Id1 + Id2 = 1000 mA, Vg12 = -0.7 V Typical



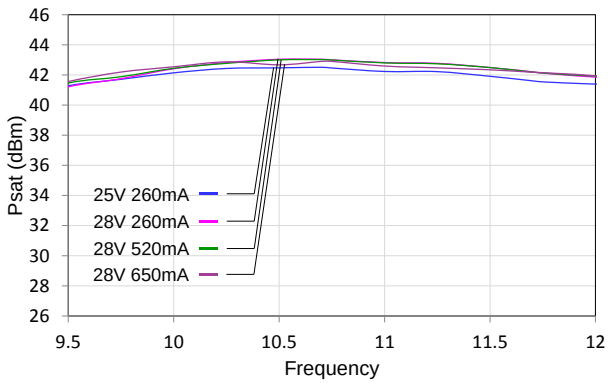
Performance Plots

Test conditions unless otherwise noted: $V_{D1} = V_{D2} = +7$ V, $I_{D1} + I_{D2} = 1000$ mA, $V_{G1} = V_{G2} = -0.7$ V, $V_{D3} = +28$ V, $I_{D3} = 260$ mA, $V_{G3} = -2.6$ V, Temp = +25 °C, $Z_0 = 50\ \Omega$

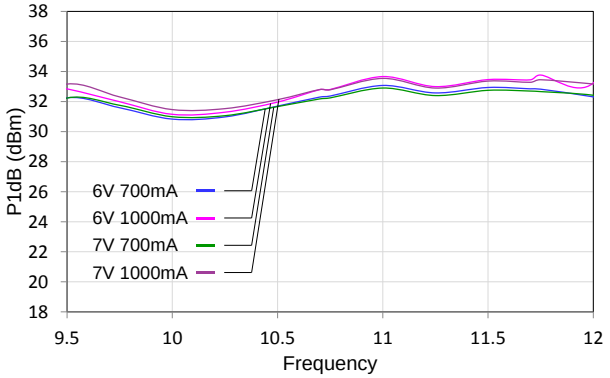
Psat vs. Frequency vs. Bias (Vd1 and Vd2)
Vd3 = 28 V, Id3 = 260 mA, Vg3 = -2.6 V Typical



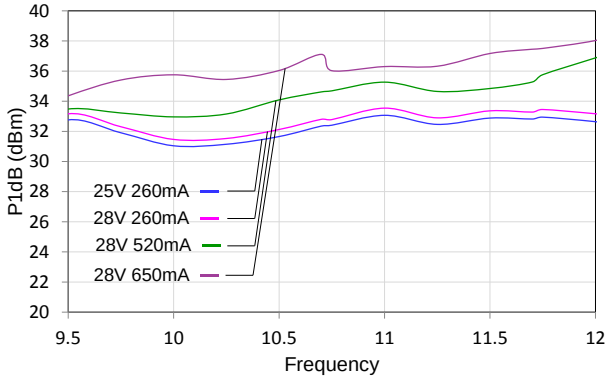
Psat vs. Frequency vs. Bias (Vd3)
Vd1 = Vd2 = 7 V, Id1 + Id2 = 1000 mA, Vg12 = -0.7 V Typical



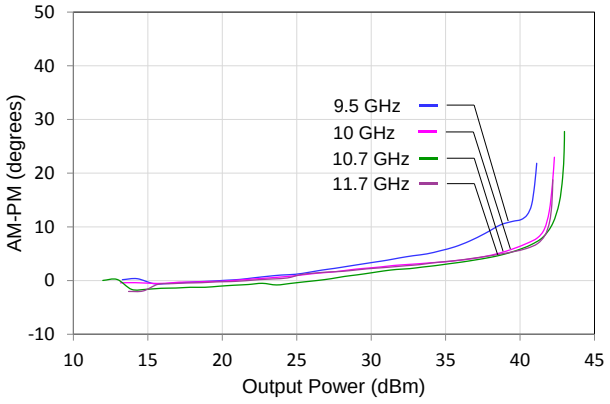
P1dB vs. Frequency vs. Bias (Vd1 and Vd2)
Vd3 = 28 V, Id3 = 260 mA, Vg3 = -2.6 V Typical



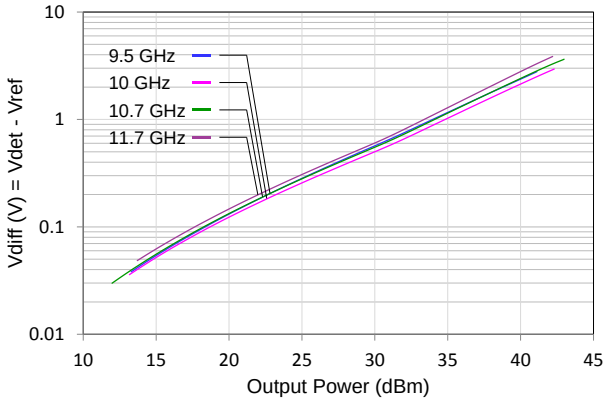
P1dB vs. Frequency vs. Bias (Vd3)
Vd1 = Vd2 = 7 V, Id1 + Id2 = 1000 mA, Vg12 = -0.7 V Typical



AM-PM vs. Pout vs. Frequency



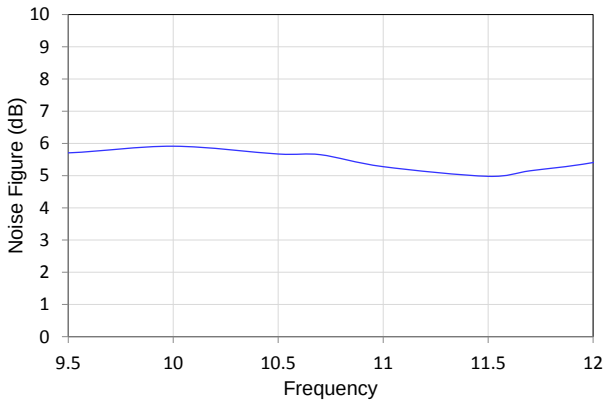
Power Detector vs. Pout vs. Frequency



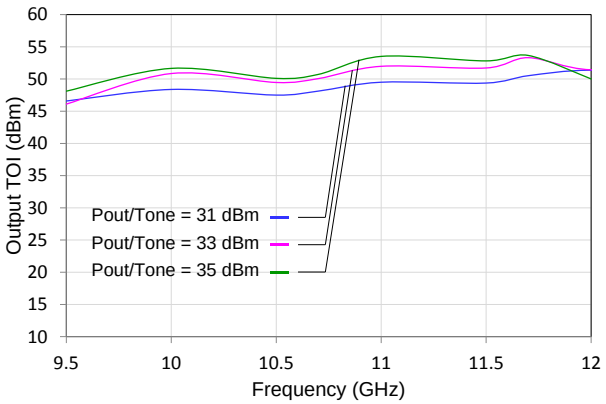
Performance Plots

Test conditions unless otherwise noted: $V_{D1} = V_{D2} = +7$ V, $I_{D1} + I_{D2} = 1000$ mA, $V_{G1} = V_{G2} = -0.7$ V, V_{D3}- = +28 V, $I_{D3} = 260$ mA, $V_{G3} = -2.6$ V, Temp = +25 °C, $Z_0 = 50\ \Omega$

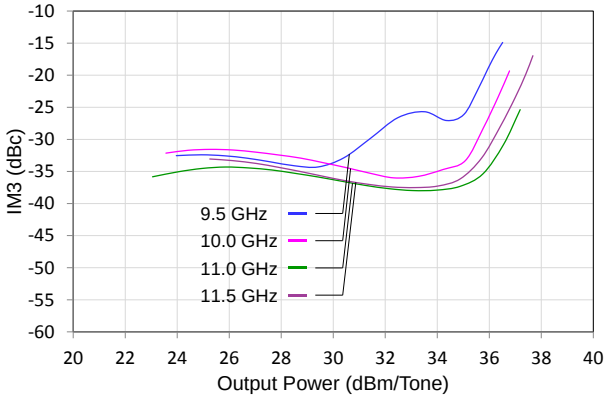
Noise Figure vs. Frequency



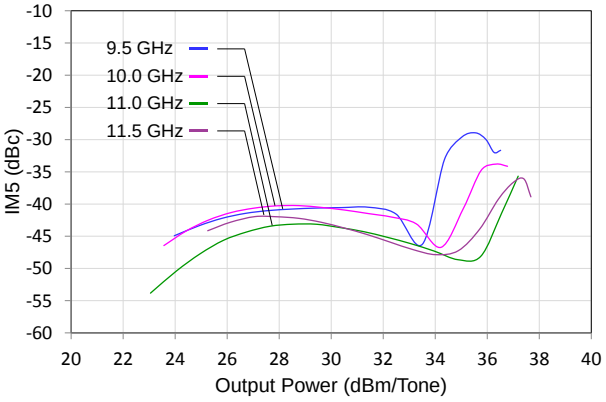
TOI vs. Frequency vs. Pout/Tone



IM3 vs. Pout/Tone vs. Frequency

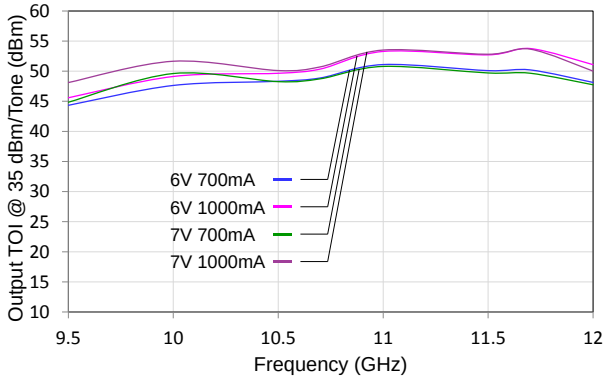


IM5 vs. Pout/Tone vs. Frequency



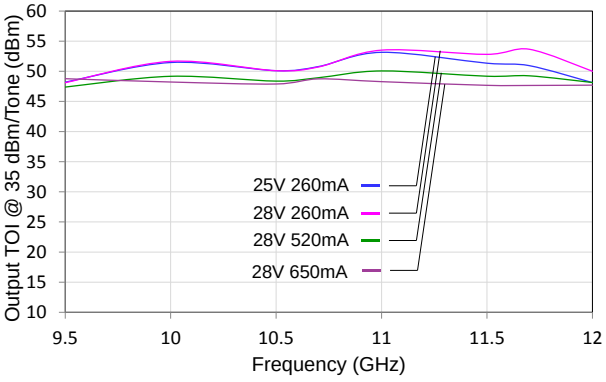
TOI vs. Frequency vs. Bias (Vd1 and Vd2)

Vd3 = 28 V, Id3 = 260 mA, Vg3 = -2.6 V Typical



TOI vs. Frequency vs. Bias (Vd3)

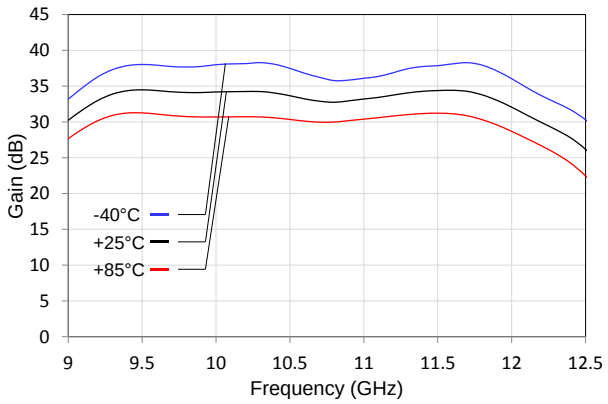
Vd1 = Vd2 = 7 V, Id1 + Id2 = 1000 mA, Vg12 = -0.7 V Typical



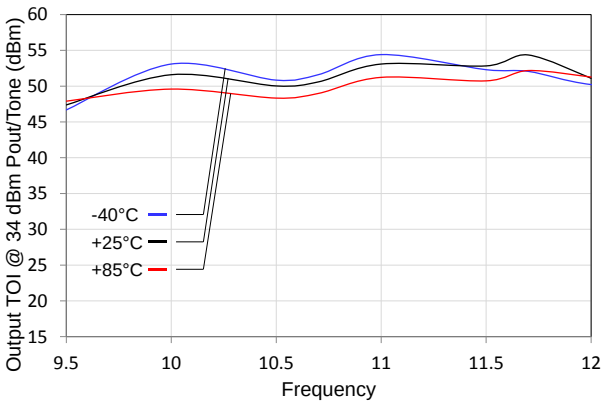
Performance Plots

Test conditions unless otherwise noted: $V_{D1} = V_{D2} = +7$ V, $I_{D1} + I_{D2} = 1000$ mA, $V_{G1} = V_{G2} = -0.7$ V, $V_{D3} = +28$ V, $I_{D3} = 260$ mA, $V_{G3} = -2.6$ V, Temp = +25 °C, $Z_0 = 50\ \Omega$

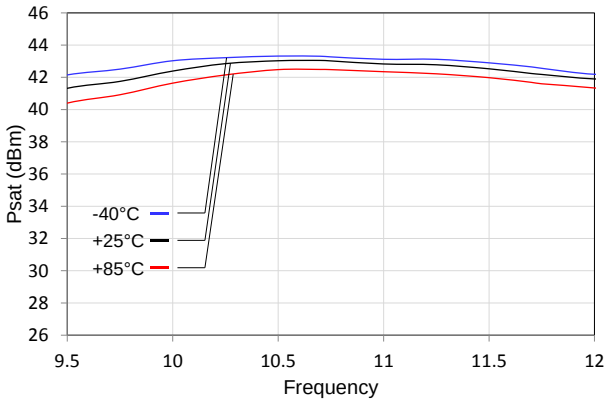
Gain vs. Frequency vs. Temperature



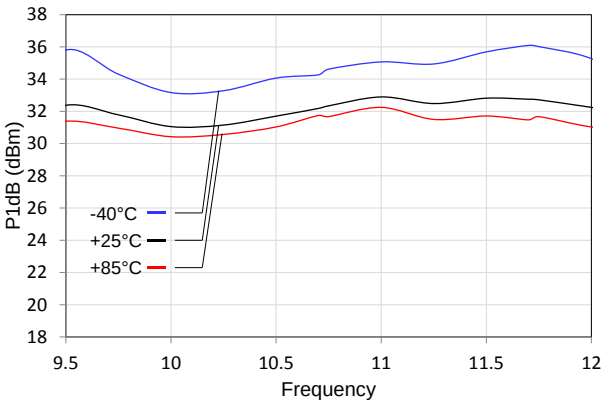
TOI vs. Frequency vs. Temperature



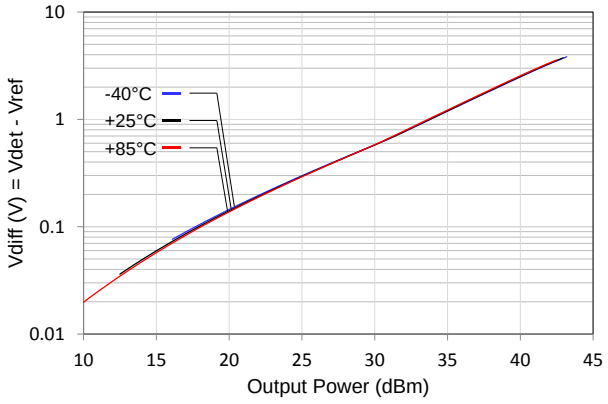
Psat vs. Frequency vs. Temperature



P1dB vs. Frequency vs. Temperature



Power Detector vs. Pout vs. Temperature



Thermal and Reliability Information (GaAs Driver Stage)

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	CW $T_{baseplate}$ = +85 °C, $V_{D\ Driver}$ = +7 V, $I_{D\ Driver}$ = 1000 mA, P_{DISS} = 7.0 W	8.14	ºC/W
Channel Temperature, T_{CH}		142	°C
Median Lifetime (T_M)		2.0×10^6	Hrs
Thermal Resistance (θ_{JC}) (1)	CW $T_{baseplate}$ = +85 °C, $V_{D\ Driver}$ = +7 V, $I_{D\ Driver}$ = 1018 mA, P_{OUT} = +39 dBm, P_{DISS} = 7.1 W	8.17	ºC/W
Channel Temperature, T_{CH} (Under RF)		143	°C
Median Lifetime (T_M)		1.8×10^6	Hrs

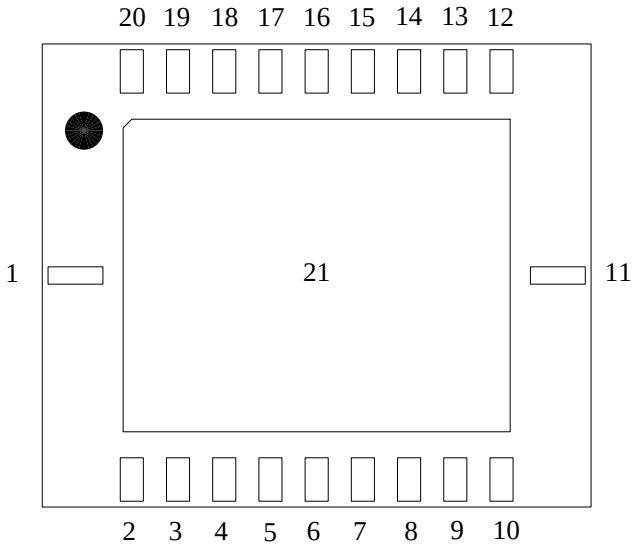
Notes:
1. Thermal resistance measured at back of package.

Thermal and Reliability Information (GaN Final Stage)

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	CW $T_{baseplate}$ = +85 °C, $V_{D\ Driver}$ = +28 V, $I_{D\ Final}$ = 260 mA, P_{DISS} = 7.3 W	3.42	ºC/W
Channel Temperature, T_{CH}		110	°C
Thermal Resistance (θ_{JC}) (1)	CW $T_{baseplate}$ = +85 °C, $V_{D\ Driver}$ = +28 V, $I_{D\ Final}$ = 930 mA, P_{OUT} = +39 dBm, P_{DISS} = 18 W	3.44	ºC/W
Channel Temperature, T_{CH} (Under RF)		147	°C

Notes:
1. Thermal resistance measured at back of package.
2. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance and Reliability Estimates

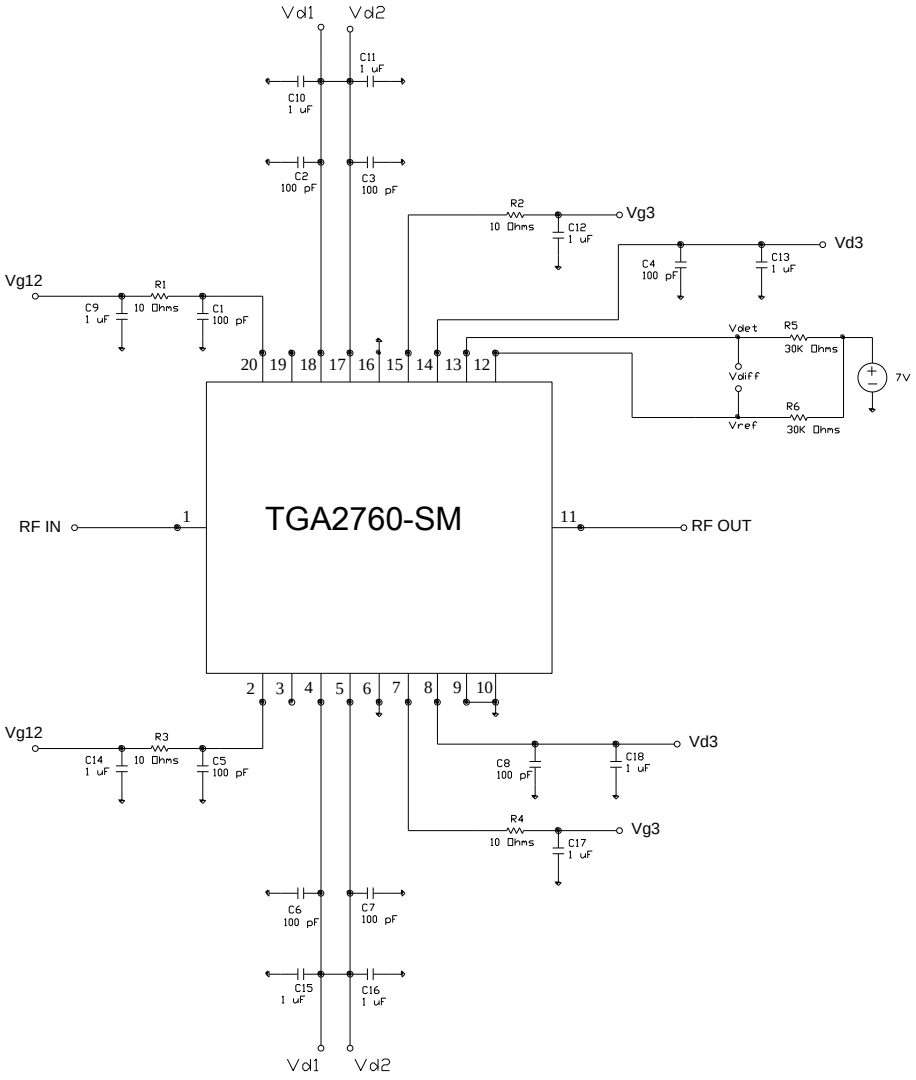
Pin Configuration and Description



Top View

Pad No.	Label	Description
1	RF IN	RF Input, matched to 50 Ω, AC Coupled.
2, 20	V_{G12}	Gate voltage. Bias network is required; can be biased from either pin, and non-biased pin can be left open; see Application Circuit on page 10 as an example.
3, 6, 9, 10, 16, 19	NC	No internal connection; can be grounded on PCB.
4, 18	V_{D1}	Drain voltage. Bias network is required; see Application Circuit on page 10 as an example.
5, 17	V_{D2}	Drain voltage. Bias network is required; see Application Circuit on page 10 as an example.
7, 15	V_{G3}	Gate voltage. Bias network is required; can be biased from either pin, and non-biased pin can be left opened; see Application Circuit on page 10 as an example.
8, 14	V_{D3}	Drain voltage. Bias network is required; see Application Circuit on page 10 as an example.
11	RF OUT	RF Output, matched to 50 ohms, AC Coupled.
12	V_{REF}	Reference diode output voltage.
13	V_{DET}	Detector diode output voltage. Varies with RF output power.
21	GND	Backside Paddle. Multiple vias should be employed to minimize inductance and thermal resistance; see Mounting Configuration on page 13 for suggested footprint.

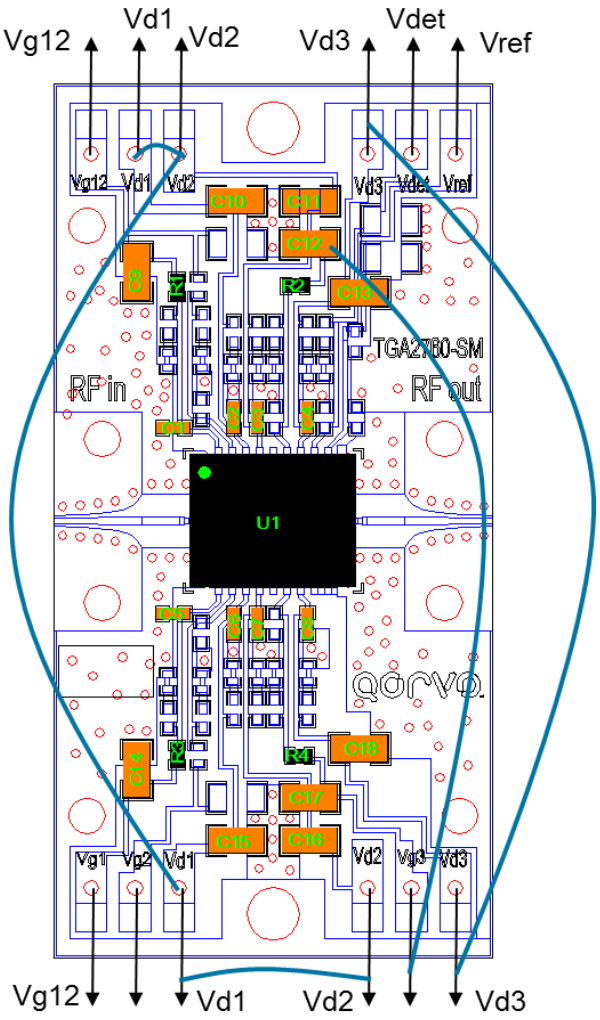
Application Circuit



V_{G12} can be biased from either side, and the non-biased side can be left open.
V_{D1}, V_{D2}, V_{D3}, must be biased from both sides.

Bias-up Procedure	Bias-down Procedure
V_{G12} set to −1.5 V	Turn off RF signal
V_{G3} set to −3.5 V	Reduce V_{G12} to −1.5 V. Ensure I_D ~ 0 mA
V_{D1}, V_{D2} set to +7 V	Reduce V_{G3} to −3.5 V. Ensure I_D ~ 0 mA
V_{D3} sets to +28 V	Turn V_{D1}, V_{D2}, V_{D3} to 0 V
Adjust V_{G12} more positive until quiescent I_D is 1000 mA. This will be ~ V_G = −0.7 V typical	Turn V_{G12}, V_{G3} to 0 V
Adjust V_{G3} more positive until quiescent I_D is 260 mA. This will be ~ V_G = −2.6 V typical	
Apply RF signal	

Application Evaluation Board



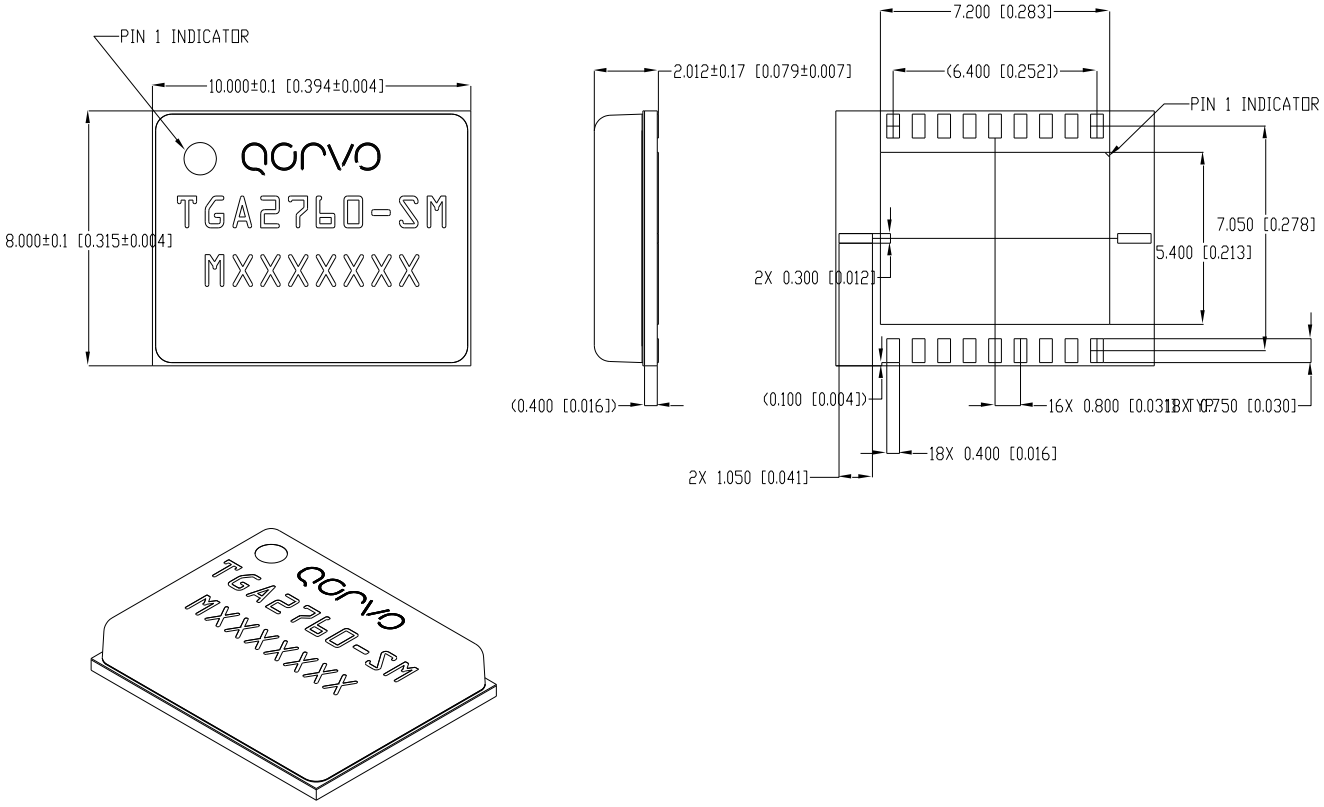
1. Board Material is RO4003 0.008” thickness with ½ oz. copper cladding

Bill of Material

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	Qorvo	
C1 – C8	100 pF	Cap, 0402, +50 V, 5%, COG	various	
C9 – C18	1 µF	Cap, 0603, +50 V, 5%, X5R	various	
R1 – R4	10 Ω	Res, 0402, 1/16W, 5%, SMD	various	
U1		9.5 – 12 GHz Power Amplifier	Qorvo	TGA2760-SM

Package Marking and Dimensions

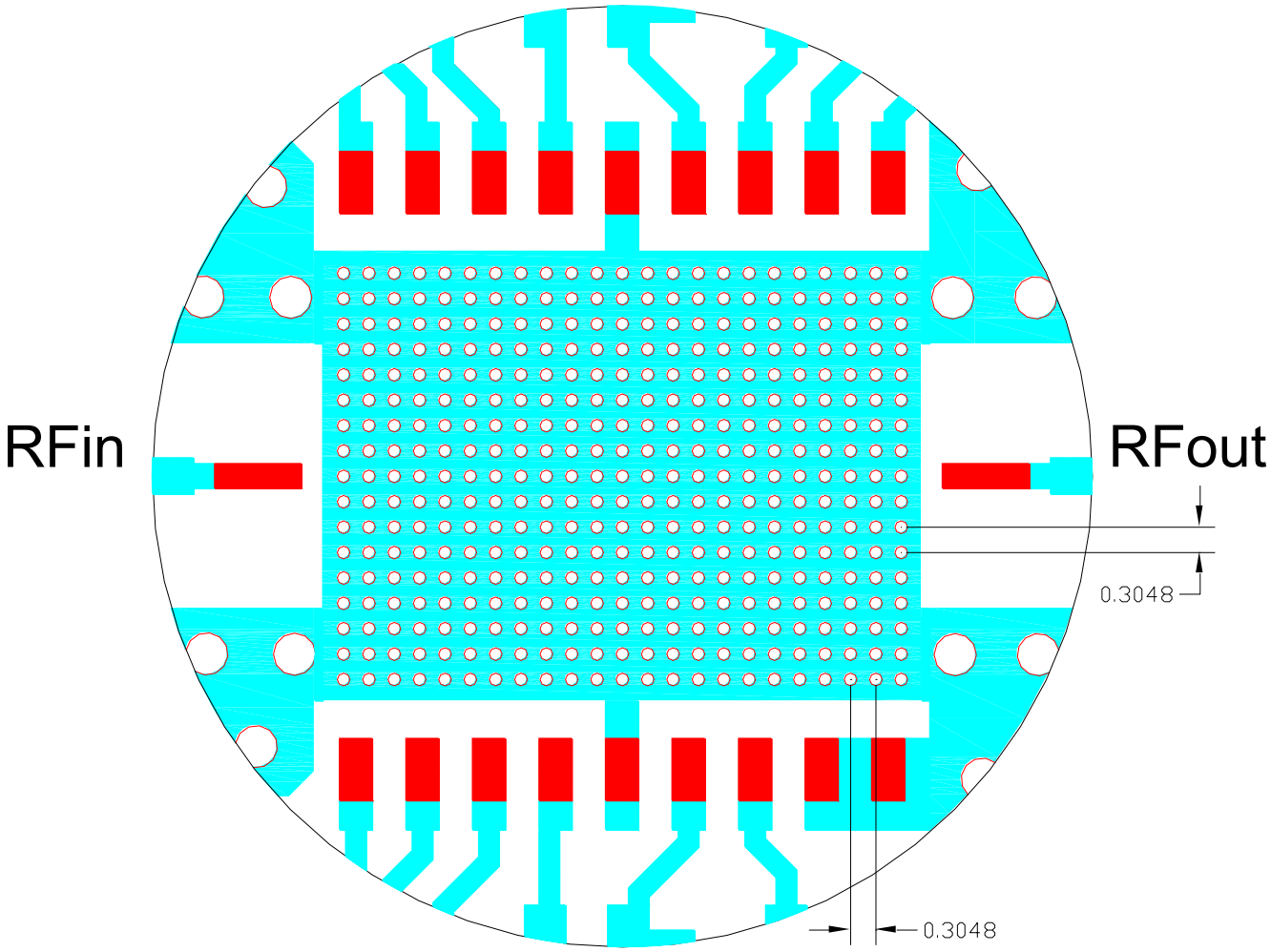
Marking: Part Number – TGA2760-SM
Lot Code – MXXXXXXX



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. This package is lead-free/RoHS-compliant with an embedded heat spreader, and the plating material on the leads is NiAu. It is compatible with both lead-free (maximum 260 °C reflow temperature) and tin-lead (maximum 245 °C reflow temperature) soldering processes.

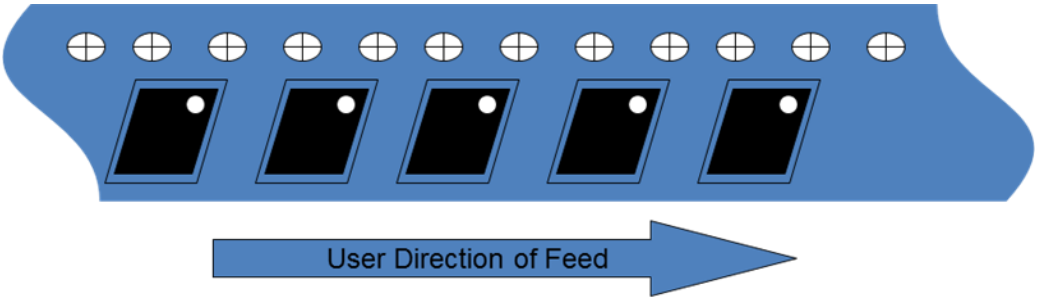
PCB Mounting Pattern



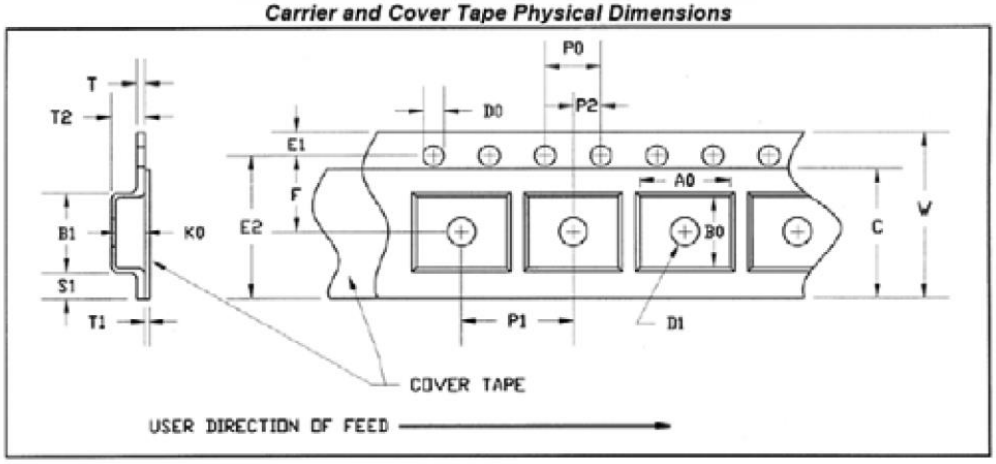
Notes:

1. The pad pattern shown has been developed and tested for optimized assembly at Qorvo. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.
2. Ground vias are critical for the proper performance of this device. Vias should have a final plated thru diameter of .1524 mm (.006”).
3. For best thermal performance, vias under the ground paddle should be copper filled.

Tape and Reel Information



Carrier and Cover Tape Physical Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.331	8.4
	Width	B0	0.409	10.4
	Depth	K0	0.094	2.4
	Pitch	P1	0.472	12.0
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.331	8.4
	Cavity to Perforation - Width Direction	F	0.409	10.4
Cover Tape	Width	C	0.472	12.0
Carrier Tape	Width	W	0.945	24.0

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1A	ESDA / JEDEC JESD22-A114
ESD – Charged Device Model (CDM)	Class C2a	JEDEC JS-002-2014
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.
Contact plating: NiAu

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com
Tel: 1-844-890-8163
Email: customer.support@qorvo.com

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