TGA2238

8 – 11 GHz 60 W GaN Power Amplifier

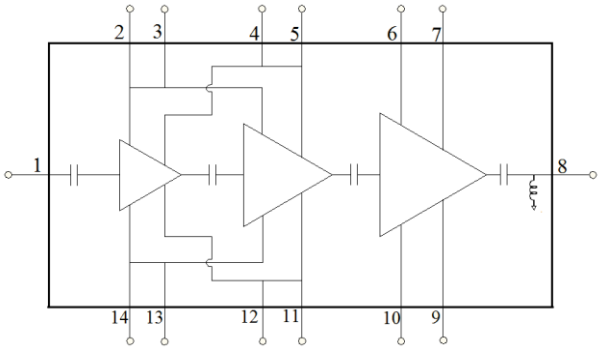
Applications

- X-band radar

Product Features

- Frequency Range: 8 – 11 GHz
- P_{OUT}: 48dBm @ P_{IN} = 23 dBm
- PAE: 42% @ P_{IN} = 23 dBm
- Large Signal Gain: 25 dB
- Small Signal Gain: 31 dB
- Return Loss: >10 dB
- Bias: V_D = 28 V, I_{DQ} = 650 mA, V_G = -2.8 V Typical
- Pulsed V_D: PW = 100 us and DC = 10%
- Chip Dimensions: 5.49 x 7.0 x 0.10 mm

Functional Block Diagram



General Description

Qorvo's TGA2238 is a high power MMIC amplifier fabricated on Qorvo's production 0.25um GaN on SiC process (QGaN25). The TGA2238 operates from 8 – 11 GHz and provides a superior combination of power, gain and efficiency by achieving more than 60 W of saturated output power with 25 dB of large signal gain and more than 42% power-added efficiency.

This superior performance provides system designers the flexibility to improve system performance while reducing size and cost.

The TGA2238 is matched to 50Ω with integrated DC blocking capacitor on RF input port simplifying system integration. It is ideally suited for military and commercial x-band radar systems.

Lead-free and RoHS compliant.

Evaluation boards are available upon request.

Pad Configuration

Pad No.	Symbol
1	RF In
2, 14	V_{G1}
3, 13	V_{G2}
4, 12	V_{D1}
5, 11	V_{D2}
6, 10	V_{G3}
7, 9	V_{D3}
8	RF Out

Ordering Information

Part	Description
TGA2238	8 – 11 GHz 60 W GaN Power Amplifier

Absolute Maximum Ratings

Parameter	Value
Drain Voltage (V_D)	40 V
Gate Voltage Range (V_G)	-8 to 0 V
Drain Current (I_D)	8 A
Gate Current (I_G)	-26 to 62 mA
Power Dissipation (P_{DISS}), 85°C, Pulsed: PW = 100us; DC = 10%	158 W
Input Power (P_{IN}) 50 Ω:, V_D = 25 V, 85 °C, Pulsed: PW = 100 us; DC = 10%	30 dBm
Input Power (P_{IN}), VSWR 3:1: V_D = 25 V, 85 °C; Pulsed: PW = 100 us; DC = 10%	30 dBm
Channel Temperature (T_{CH})	275 °C
Mounting Temperature (30 seconds)	320 °C
Storage Temperature	-55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value
Drain Voltage (V_D)	28 V
Drain Current (I_{DQ})	650 mA (Total)
Gate Voltage (V_G)	-2.8 V (Typ.)

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

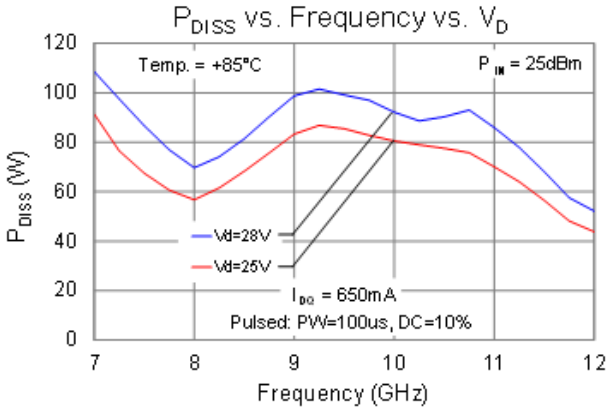
Test conditions unless otherwise noted: 25°C , V_D = 28V, I_{DQ} = 650mA, V_G = -2.8V Typical, Pulsed V_D: PW = 100us, DC = 10%

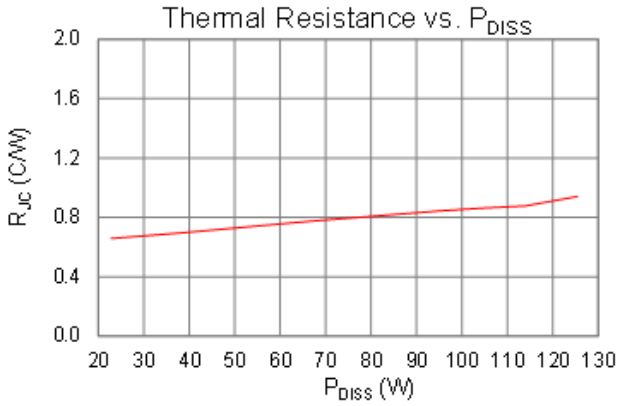
Parameter	Min	Typical	Max	Units
Operational Frequency Range	8		11	GHz
Small Signal Gain		31		dB
Input Return Loss		15		dB
Output Return Loss		15		dB
Power Gain (Pin = 23 dBm)		25		dB
Output Power (Pin = 23 dBm)		48		dBm
Power Added Efficiency (Pin = 23 dBm)		42		%
Power @ 1dB Compression (P1dB)		36		dBm
Small Signal Gain Temperature Coefficient		-0.058		dB/°C
Output Power Temperature Coefficient		-0.014		dBm/°C

Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, Pulsed V_D: PW = 100 us, DC = 10%, V_D = 25 V, I_{D_Drive} = 6 A, Freq = 9.25 GHz P_{IN} =25 dBm, P_{OUT} = 47.8 dBm, P_{DISS} = 92 W	0.57	ºC/W
Channel Temperature (T_{CH}) (Under RF drive)		137	°C
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, Pulsed V_D: PW = 100 us, DC = 10% V_D = 28 V, I_{D_Drive} = 6.3 A, Freq = 9.25 GHz P_{IN} = 25 dBm, P_{OUT} = 48.3 dBm, P_{DISS} = 107 W	0.58	ºC/W
Channel Temperature (T_{CH}) (Under RF drive)		147	°C

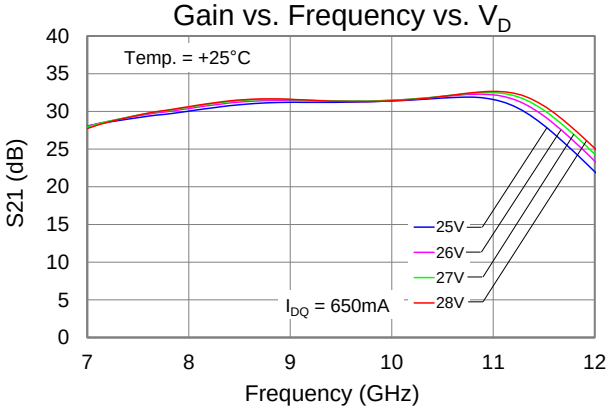
Notes:
1. Thermal resistance determined to the back of a 20 mil Cu-Mo carrier plate with eutectic die attach (85 °C)
2. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates



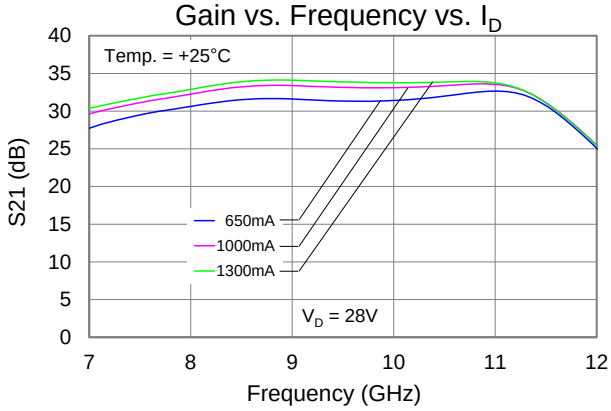


Typical Performance (Small Signal)

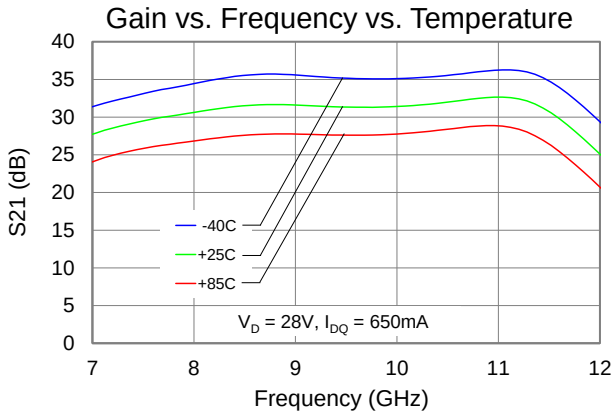
Gain vs. Frequency vs. V_D



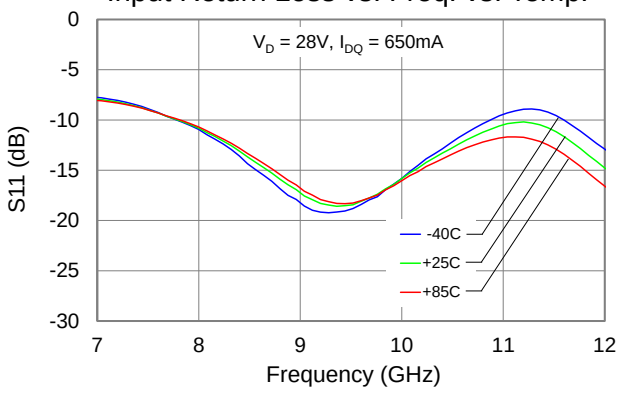
Gain vs. Frequency vs. I_D



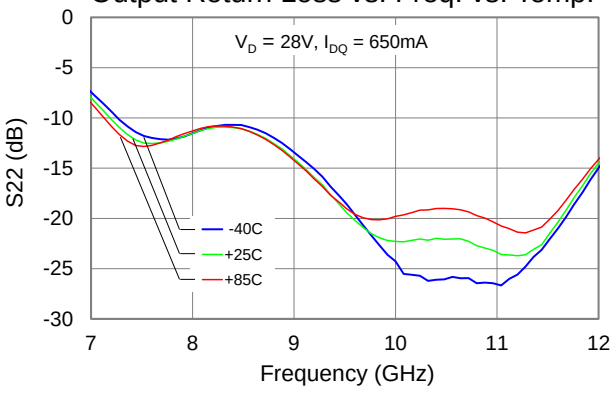
Gain vs. Frequency vs. Temperature



Input Return Loss vs. Freq. vs. Temp.

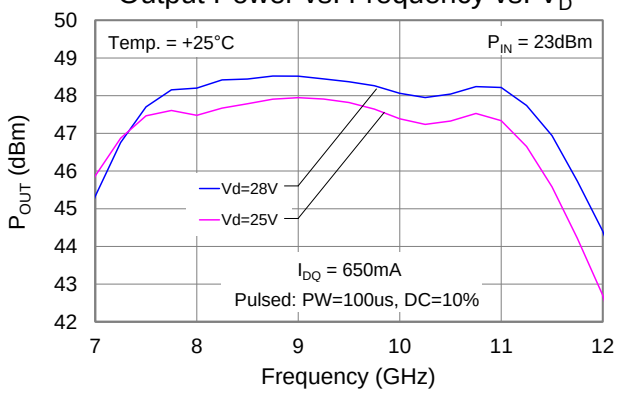


Output Return Loss vs. Freq. vs. Temp.

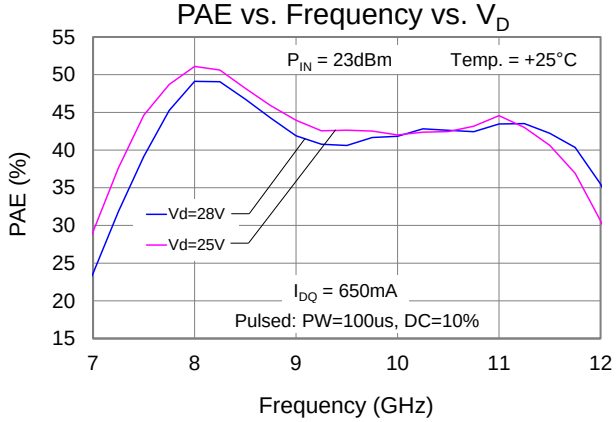


Typical Performance (Pulsed Operation)

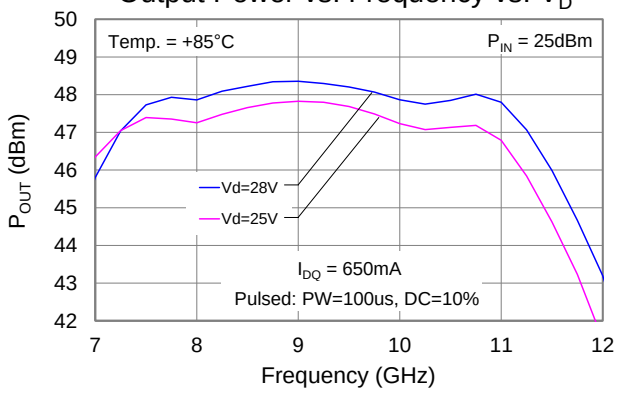
Output Power vs. Frequency vs. V_D



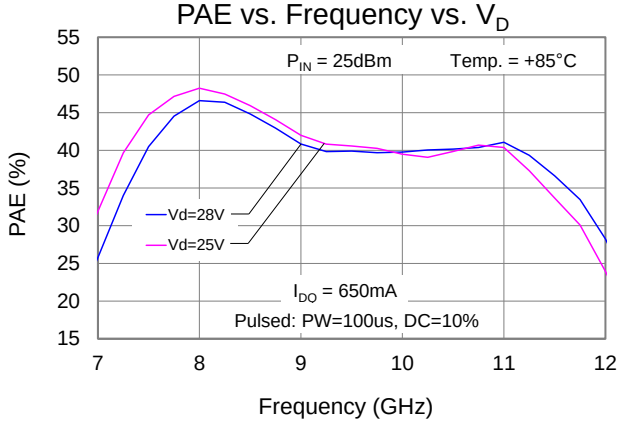
PAE vs. Frequency vs. V_D



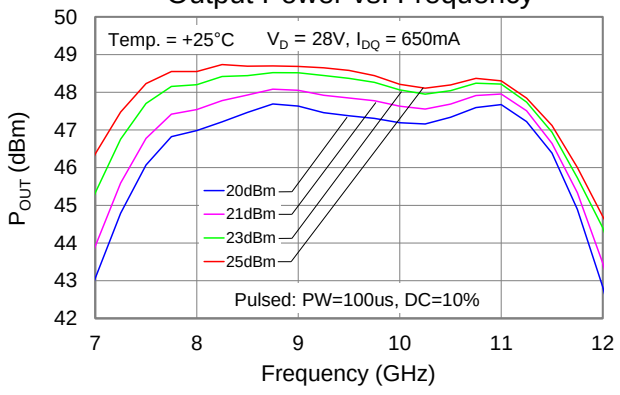
Output Power vs. Frequency vs. V_D



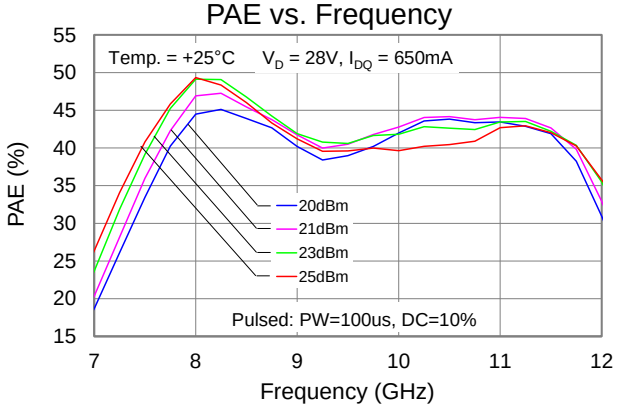
PAE vs. Frequency vs. V_D



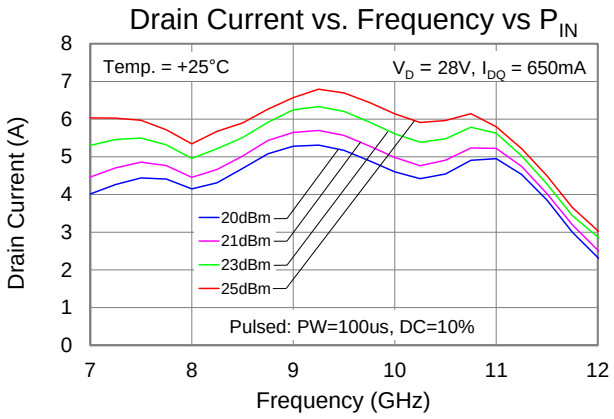
Output Power vs. Frequency

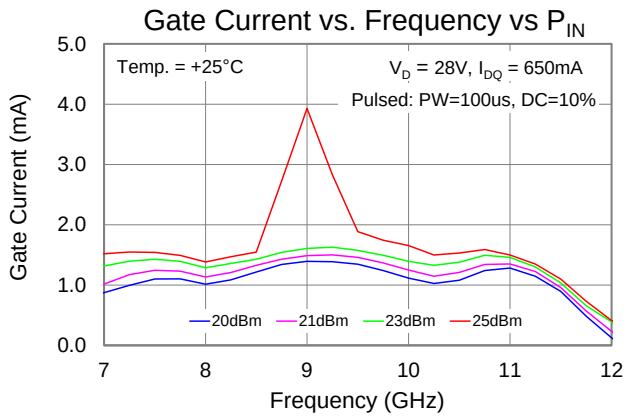


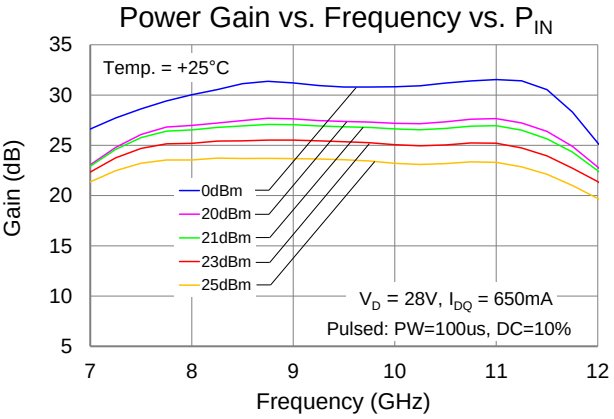
PAE vs. Frequency

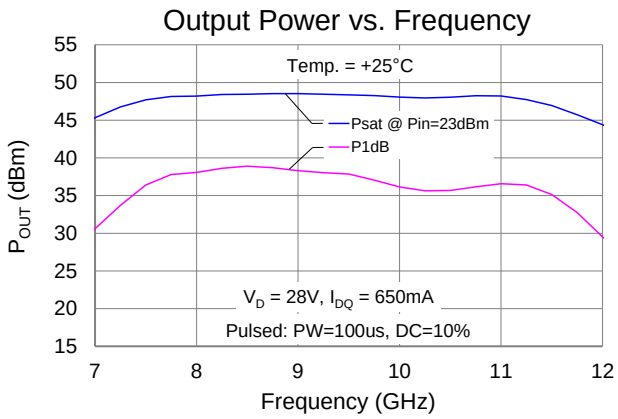


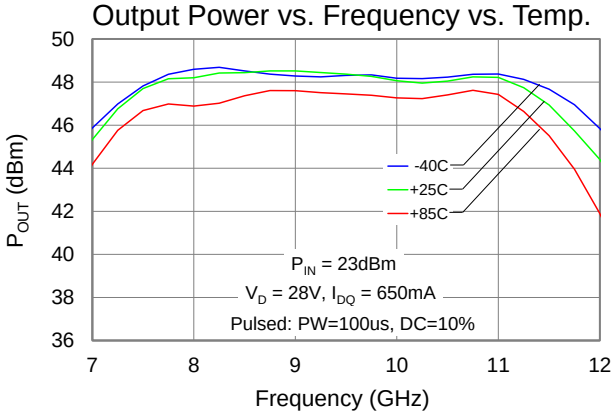
Typical Performance (Pulsed Operation)

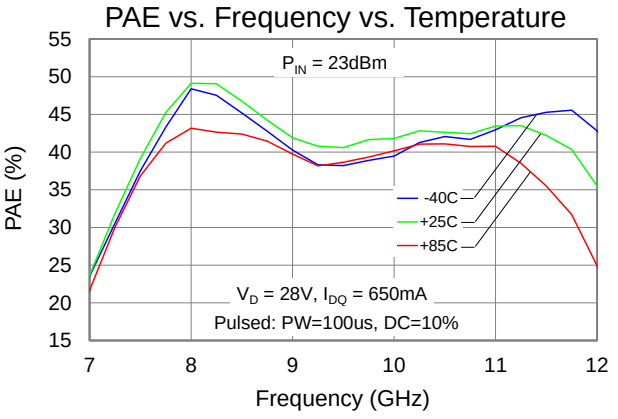






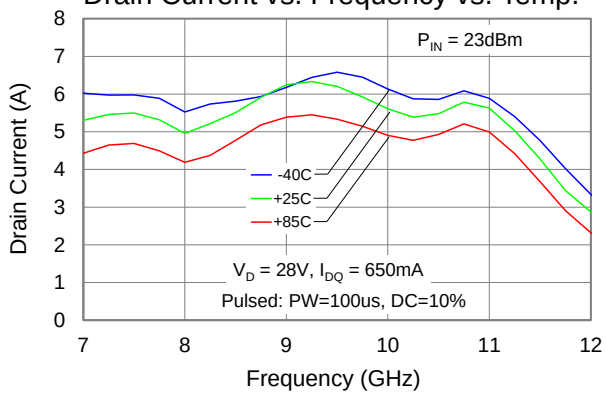




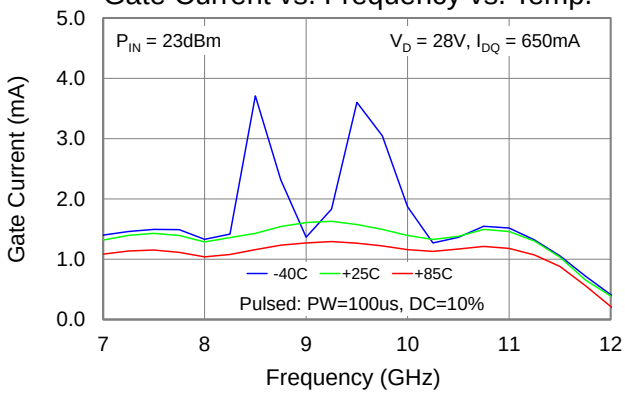


Typical Performance (Pulsed Operation)

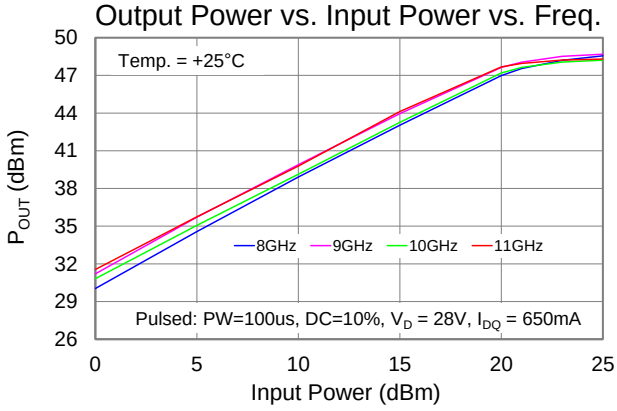
Drain Current vs. Frequency vs. Temp.



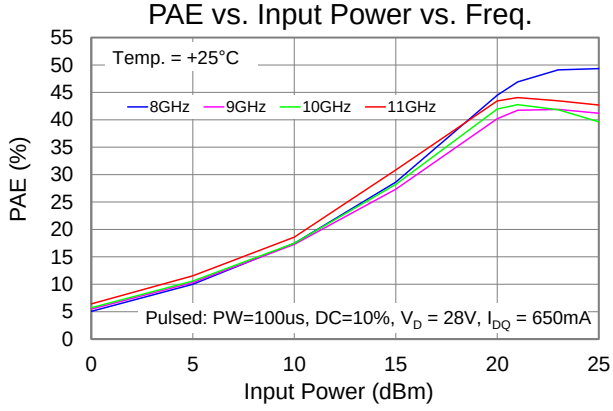
Gate Current vs. Frequency vs. Temp.



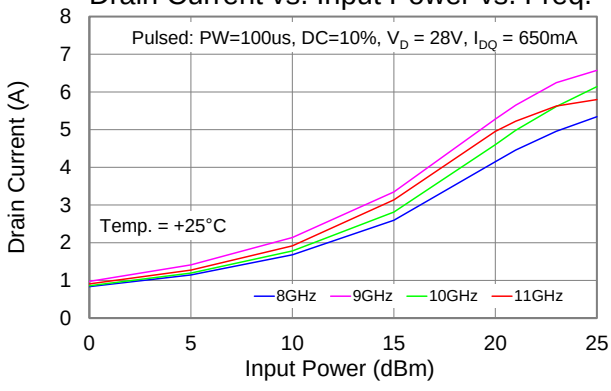
Output Power vs. Input Power vs. Freq.



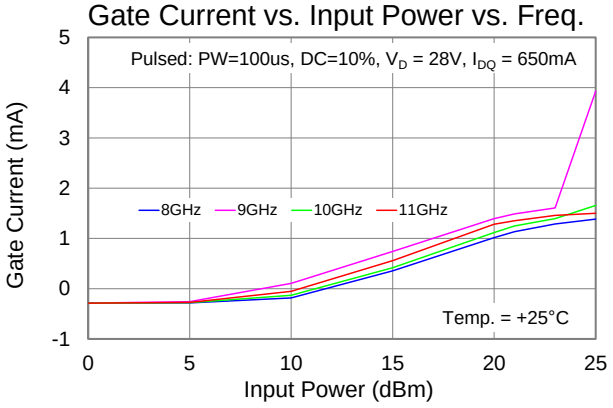
PAE vs. Input Power vs. Freq.



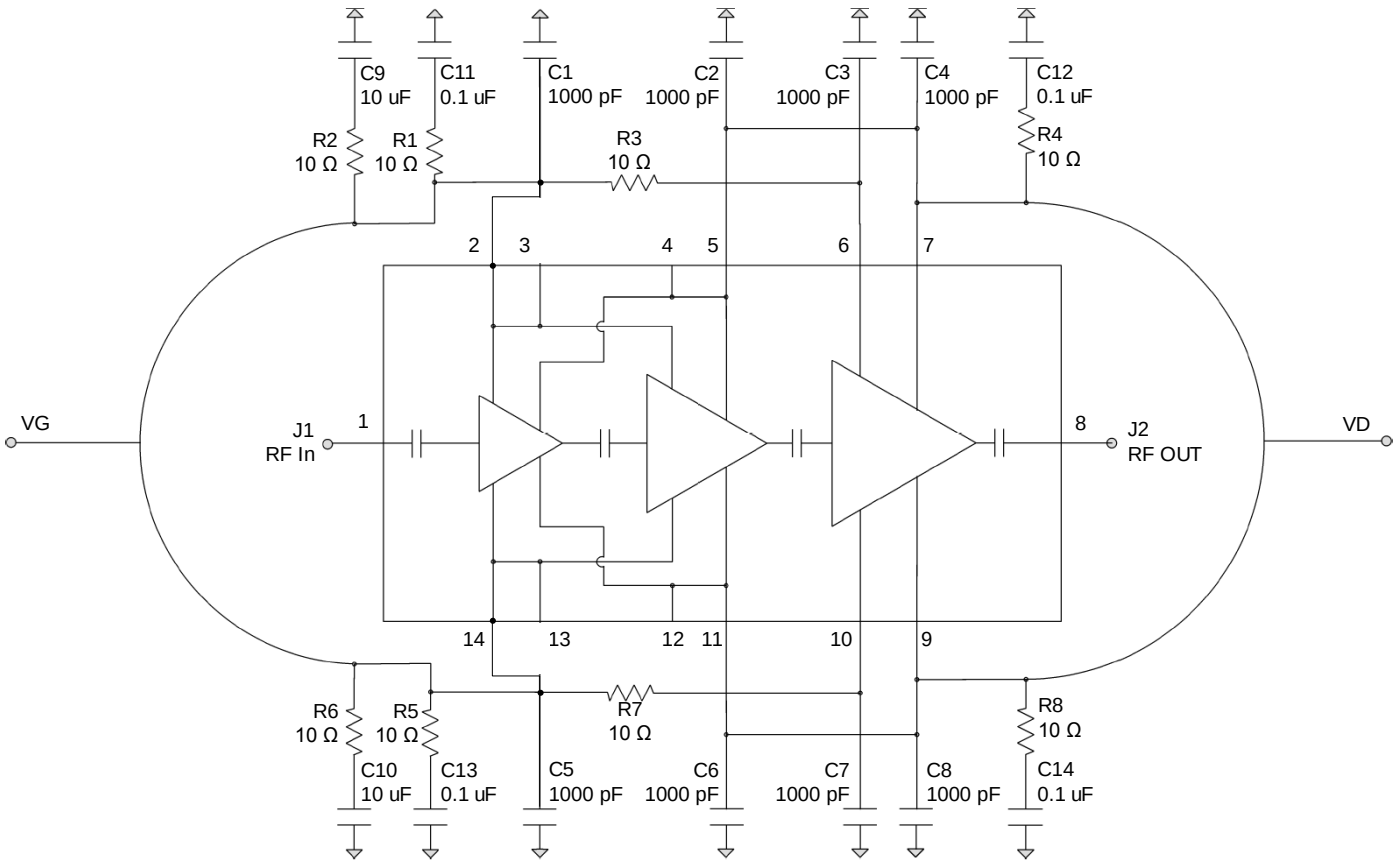
Drain Current vs. Input Power vs. Freq.



Gate Current vs. Input Power vs. Freq.



Application Circuit



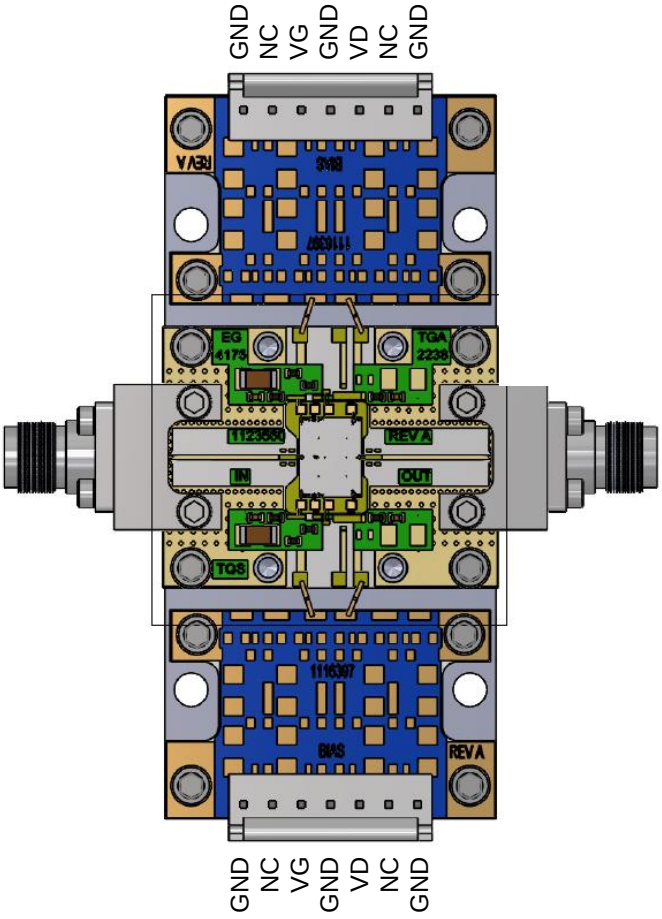
Bias-up Procedure

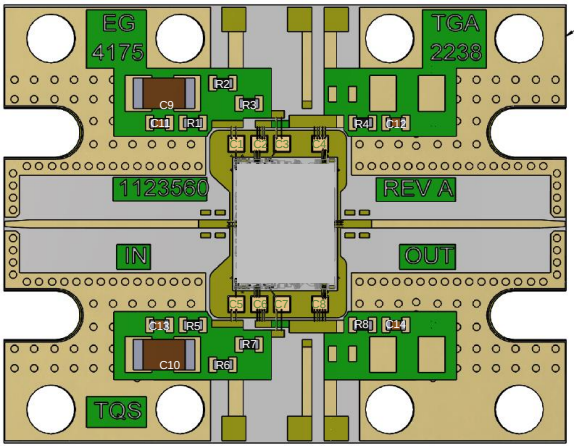
1. Set I_D limit to 8A, I_G limit to 20mA
2. Set V_G to -5.0V
3. Set V_D +28V
4. Adjust V_G more positive until I_{DQ} = 650mA (V_G ~ -2.8V Typical)
5. Apply RF signal

Bias-down Procedure

1. Turn off RF signal
2. Reduce V_G to -5.0V. Ensure I_{DQ} ~ 0mA
3. Set V_D to 0V
4. Turn off V_D supply
5. Turn off V_G supply

Evaluation Board (EVB) Layout Assembly

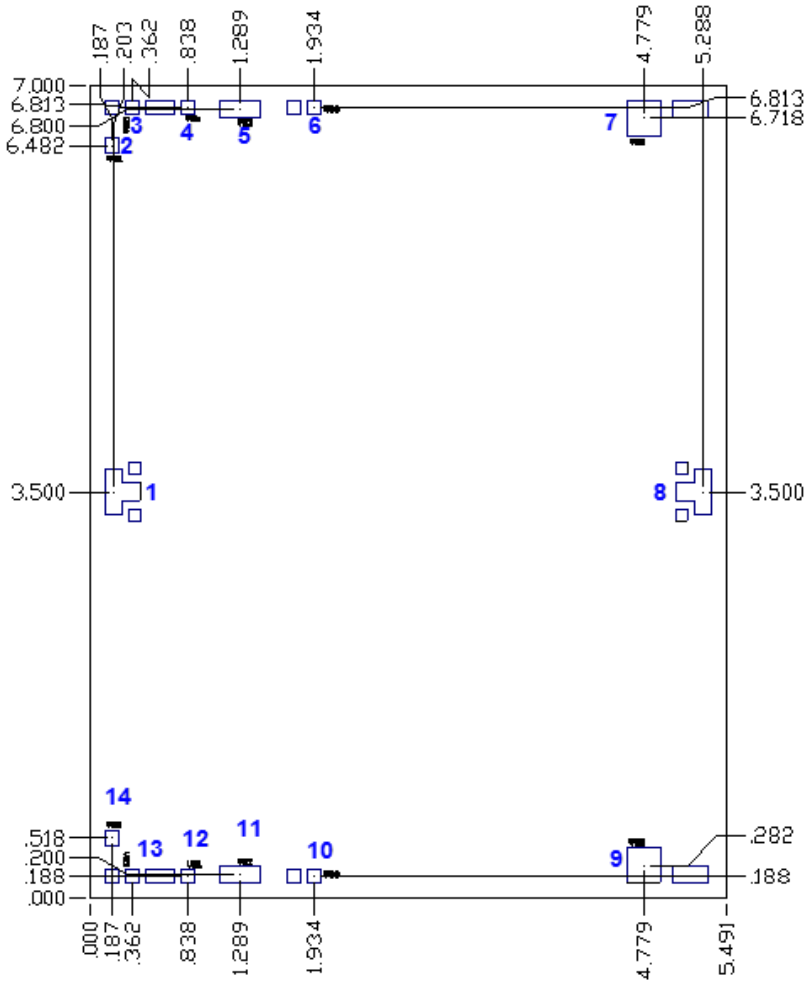




Bill of Materials

Ref. Des.	Value	Description	Manufacturer	Part Number
C1 – C8	1000 pF	CAP, 1000 Pf, 10%, 50V, BORDER, SL	Various	
C9 – C10	0.1 uF	CAP, 10 Uf, 20%, 50V, x5r, 1206	Various	
C11 – C14	10 uF	Cap, 0.1 Uf, 10%, 50V, x7r, 0402	Various	
R1 – R8	10 Ω	Res, 10 ohm, 5%, 0.1 w, 0402	Various	

Mechanical Drawing & Bond Pad Description



Unit: millimeters
Thickness: 0.10
Die x, y size tolerance: +/- 0.050
Chip edge to bond pad dimensions are shown to center of pad
Ground is backside of die

Bond Pad	Symbol	Pad Size	Description
1	RF In	0.146 x 0.386	RF Input; matched to 50Ω; DC blocked
2, 14	VG1	0.121 x 0.121	VG1 and VG2 are internally connected so either one can be used for both VG1 or VG2, bias network is required; see Application Circuit on page 8 as an example.
3, 13	VG2	0.121 x 0.121	
4, 12	VD1	0.121 x 0.121	VD1 and VD2 are internally connected so either one can be used for both VD1 or VD2, bias network is required; see Application Circuit on page 8 as an example.
5, 11	VD2	0.346 x 0.146	
6, 10	VG3	0.121 x 0.121	VG3, bias network is required; see Application Circuit on page 8 as an example.
7, 9	VD3	0.296 x 0.310	VD 3, bias network is required; see Application Circuit on page 8 as an example.
8	RF Out	0.146 x 0.386	RF Output; matched to 50Ω; DC shorted to ground

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300°C to 3-4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: TBD
Value: TBD
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

Solderability

Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3-4 minutes, maximum.

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Email: customer.support@qorvo.com

Important Notice

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