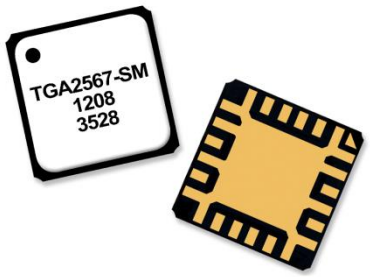
TGA2567-SM

2 – 20 GHz LNA Amplifier



QFN 4x4 mm 24L

Product Description

Qorvo's TGA2567-SM is a LNA Gain Block fabricated on Qorvo's proven 0.15um pHEMT production process.

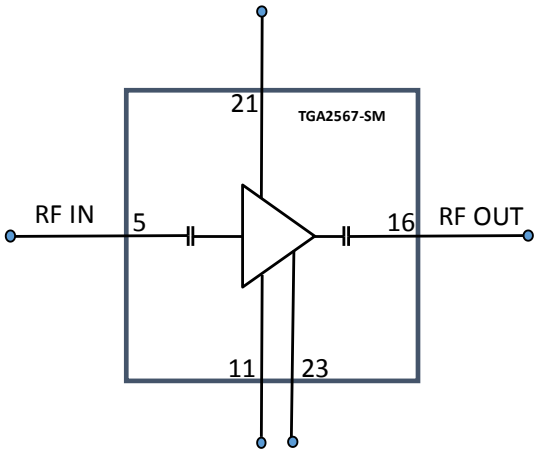
The TGA2567-SM operates from 2 to 20 GHz and typically provides 19 dBm of 1dB compressed output power with 17 dB of small signal gain. Greater than 16 dB of adjustable gain can be achieved by varying V_{G2}. The Noise Figure is typically 2 dB at mid band

The TGA2567-SM is available in a low-cost, surface mount 24 lead 4x4 AIN QFN package base with an Air cavity LCP lid. TGA2567-SM is ideally suited to support both commercial and defense related applications.

Lead-free and RoHS compliant.

Evaluation boards are available upon request.

Functional Block Diagram



Product Features

- Frequency Range: 2 – 20 GHz
- P_{SAT}: 22 dBm
- P_{1dB}: 19 dBm
- Small Signal Gain: 17 dB
- Adjustable Gain Range (using V_{G2})
- Noise Figure: 2 dB
- OIP3: 29 dBm
- Bias: V_D = 5 V, I_D = 100 mA, V_{G1} = -0.7 V typical, V_{G2} = +1.3 V
- ESD Protection Circuitry on V_D, V_{G1} and V_{G2}
- Package dimensions: 4.00 x 4.00 x 1.42 mm

Applications

- General Purpose LNA/Gain Block
- Point to Point Radio
- Electronic Warfare
- Military & Commercial Radar
- Communications

Ordering Information

Part No.	ECCN	Description
TGA2567-SM	EAR99	2 – 20 GHz LNA / Gain Block

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	6 V
Drain to Gate Voltage (V_D-V_{G1})	8 V
Gate Voltage Range (V_{G1})	−2 to 1 V
Gate Voltage Range (V_{G2})	−2 to +4 V
Drain Current (I_D)	160 mA
Gate Current Range (I_{G1}, I_{G2})	-1 to +40 mA
Power Dissipation (P_{DISS})	2.8 W
RF Input Power, CW, 50 Ω, T =25 °C	+22 dBm
Channel Temperature (T_{CH})	200 °C
Mounting Temperature (30 Seconds)	260 °C
Storage Temperature	−55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating

Parameter	Value / Range
Drain Voltage (V_D)	5 V
Drain Current (I_{DQ})	100 mA
Gate Voltage (V_{G1})[1], typical	-0.7 V
Gate Voltage (V_{G2})	+1.3 V
Operating Temperature Range (T_{BASE})	−40 to 85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Note:

[1] Adjust V_{G1} to achieve the required I_{DQ}.

Electrical Specifications

Parameter	Min	Typ	Max	Units
Operational Frequency Range	2	–	20	GHz
Small Signal Gain	–	17	–	dB
Input Return Loss	–	15	–	dB
Output Return Loss	–	14	–	dB
Noise Figure: 2 GHz	–	2.8	–	dB
Output TOI	–	29	–	dBm
Output Power (Saturation; P_{IN} = 10 dBm)	–	22	–	dBm
Output Power (1 dB Compression)	–	19	–	dBm
Small Signal Gain Temperature Coefficient	–	-0.013	–	dB/°C
Noise Figure Temperature Coefficient	–	0.009	–	dB/°C

Test conditions unless otherwise noted: 25 °C, V_D = +5 V, I_{DQ} = 100 mA, V_{G1} = −0.7 V Typical, V_{G2} = 1.3 V

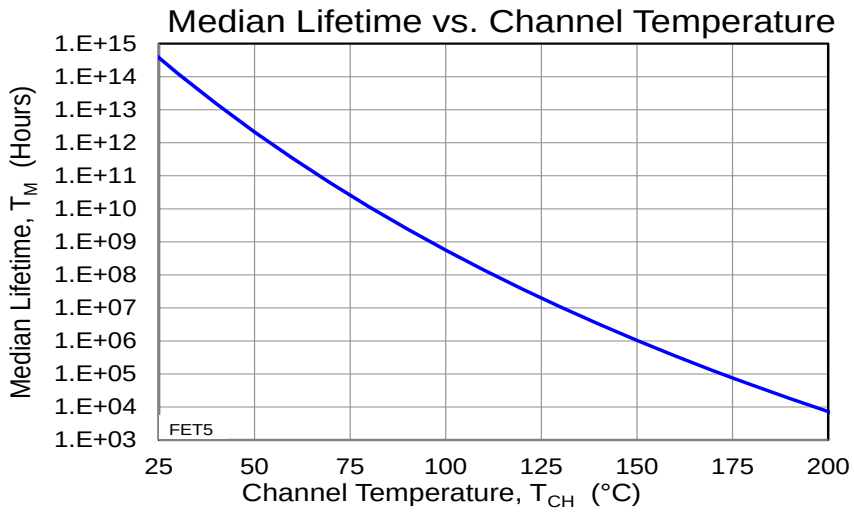
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance, θ_{JC} (1)	Tbaseplate = 85 °C	41	ºC/W
Channel Temperature, T_{CH} (Without RF Drive)	Tbaseplate = 85 °C, V_D = 5 V, I_{DQ} = 100 mA, P_{DISS} = 0.5 W	106	°C
Median Lifetime, T_M (Without RF Drive)		2.4 x 10^8	Hrs
Channel Temperature, T_{CH} (Under RF Drive)	Tbaseplate = 85 °C, V_D = 5 V, I_{DD} = 156 mA, P_{OUT} = 22.8 dBm, P_{DISS} = 0.59 W	109	°C
Median Lifetime, T_M (Under RF Drive)		1.6 x 10^8	Hrs

Notes: (1) Thermal resistance measured to back of package.

Median Lifetime

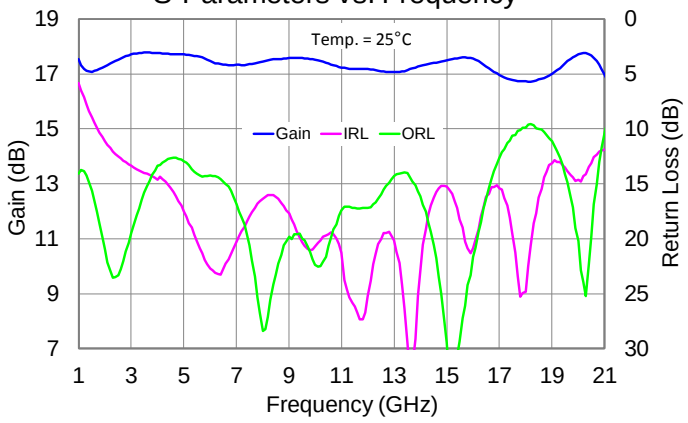
Test Conditions: V_D = 6 V; Failure Criteria = 10 % reduction in ID_MAX during DC Testing



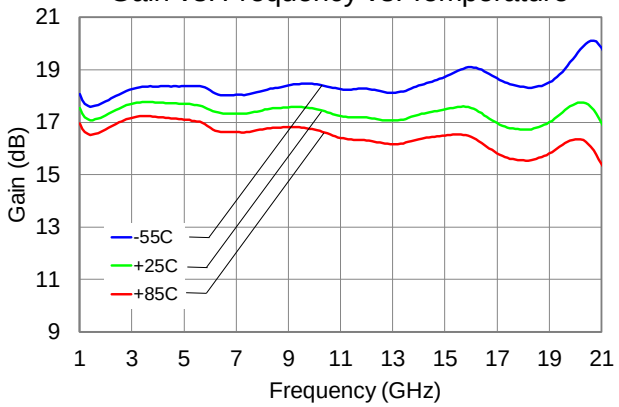
Performance Plots – Small Signal & Noise Figure

Conditions unless otherwise specified: V_D = 5 V, I_{DQ} = 100 mA, V_{G1} = -0.7 V Typical, V_{G2} = 1.3 V

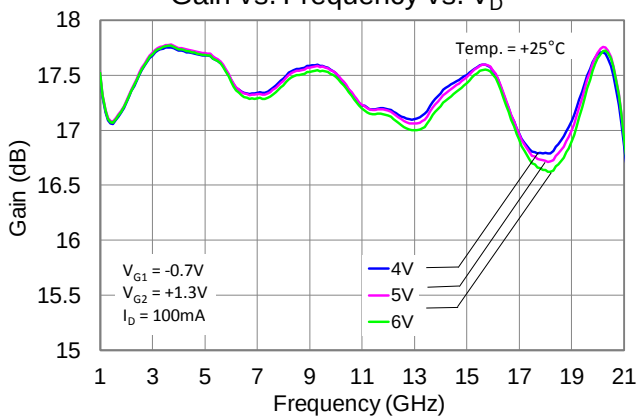
S-Parameters vs. Frequency



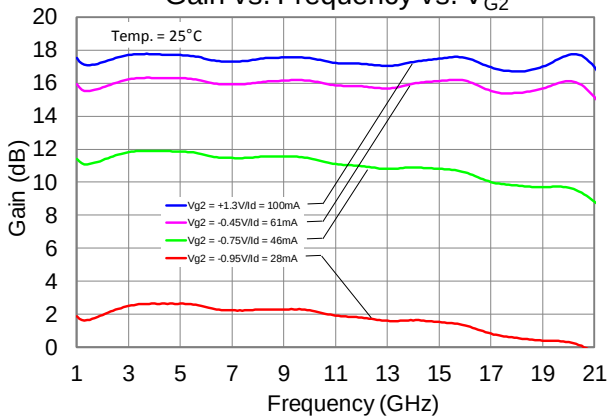
Gain vs. Frequency vs. Temperature



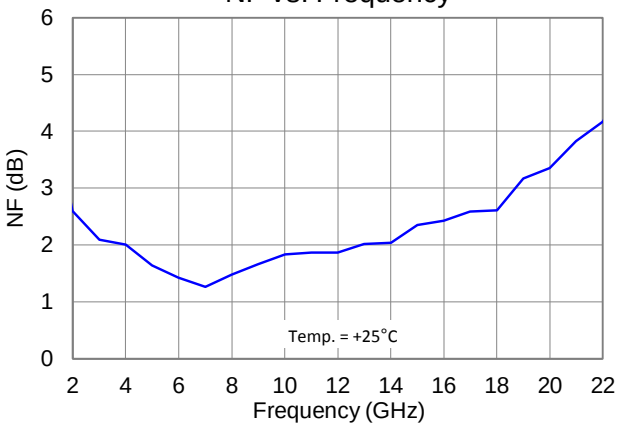
Gain vs. Frequency vs. V_D



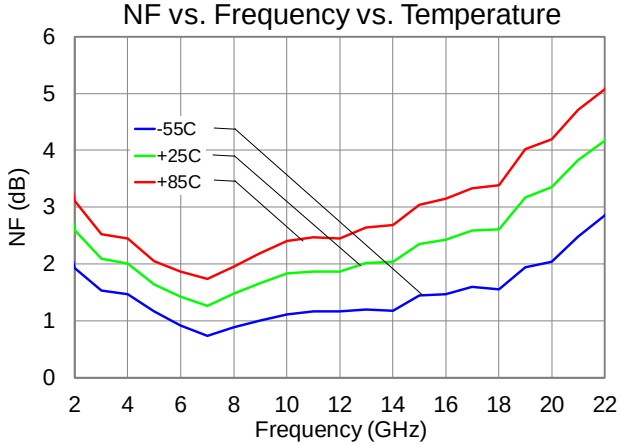
Gain vs. Frequency vs. V_{G2}



NF vs. Frequency



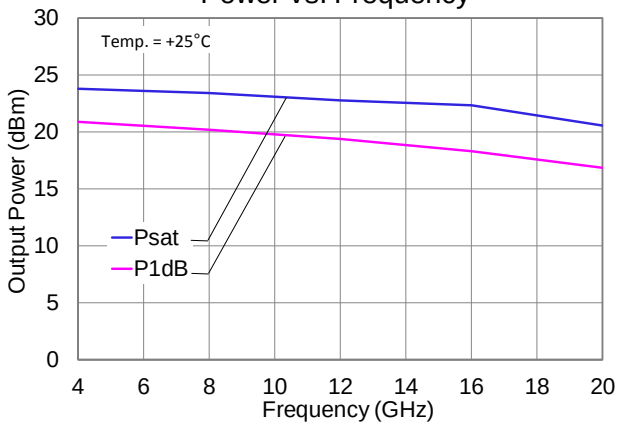
NF vs. Frequency vs. Temperature



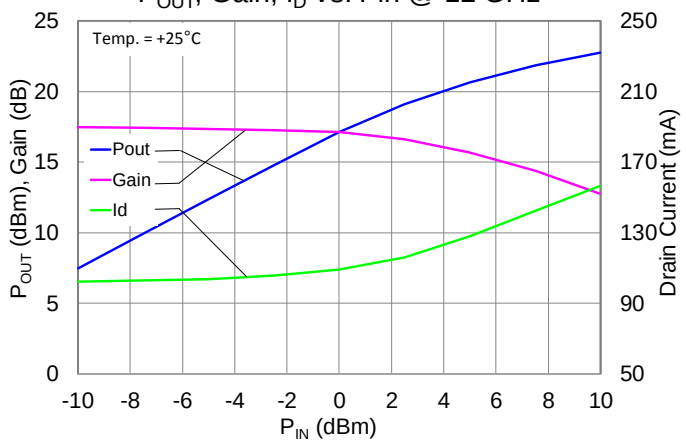
Performance Plots – Large Signal & Linearity

Conditions unless otherwise specified: V_D = 5 V, I_{DQ} = 100 mA, V_{G1} = -0.7 V Typical, V_{G2} = 1.3 V

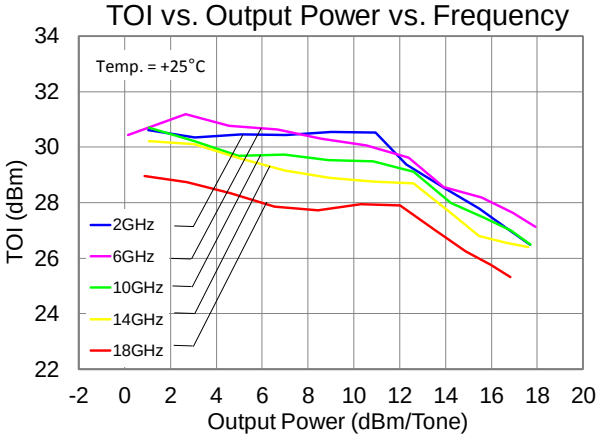
Power vs. Frequency



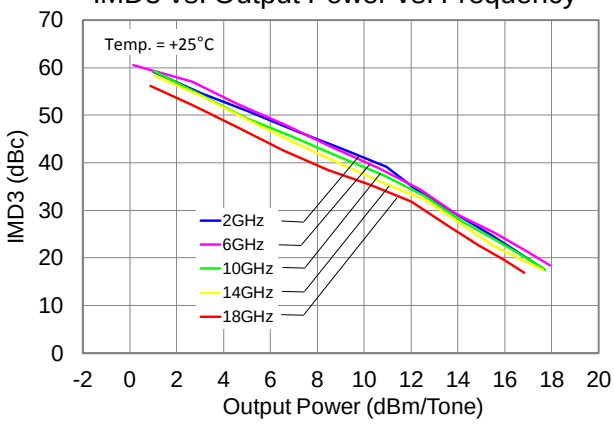
P_{OUT}, Gain, I_D vs. Pin @ 12 GHz



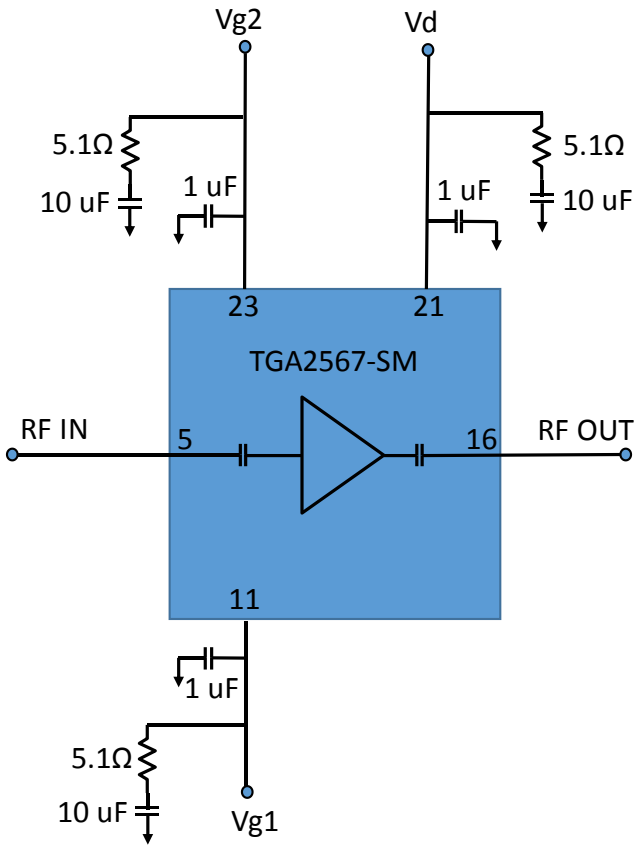
TOI vs. Output Power vs. Frequency



IMD3 vs. Output Power vs. Frequency



Applications Information



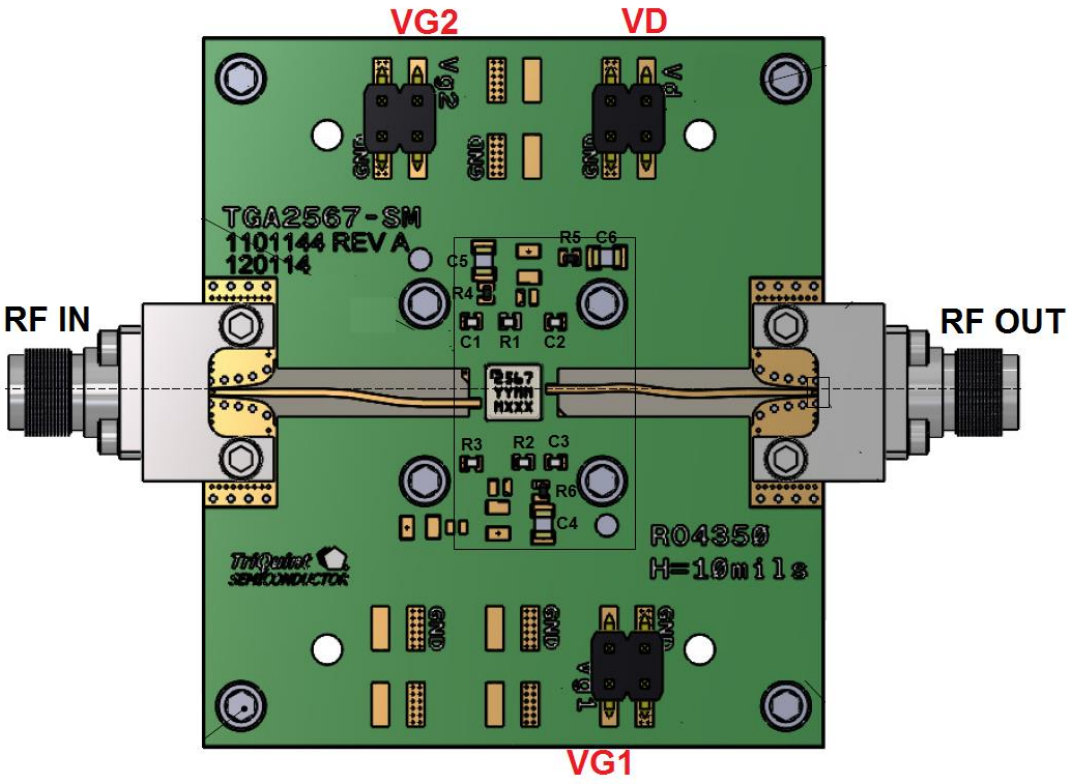
Bias Up Procedure

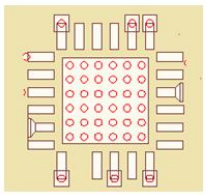
1. Set I_D limit to 160 mA, I_G limit to 24 mA
2. Apply −1.5 V to V_{G1}
3. Apply +5 V to V_D; ensure I_{DQ} is approx. 0 mA
4. Apply +1.3 V to V_{G2}
5. Adjust V_{G1} until I_{DQ} = 100 mA (V_{G1} ~ −0.7 V Typ.)
6. Adjust V_{G2} to obtain desired gain
7. Turn on RF supply

Bias Down Procedure

1. Turn off RF supply
2. Reduce V_{G1} to −1.5 V; ensure I_{DQ} is approx. 0 mA
3. Set V_{G2} to 0 V
4. Set V_D to 0 V
5. Turn off V_D supply
6. Turn off V_{G1} and V_{G2} supplies

Evaluation Board Layout Assembly and Mounting Pattern





Mounting Detail

Top dielectric material is ROGERS 4350, 0.010 inch thickness with 0.5 oz copper.

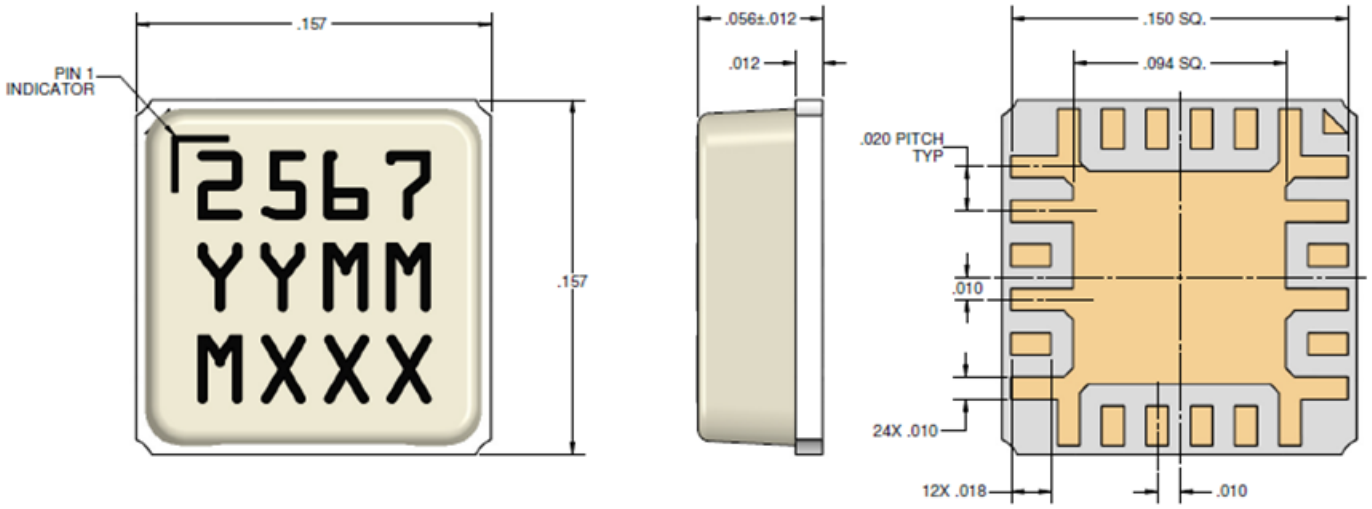
The pad pattern shown above has been developed and tested for optimized assembly at Qorvo. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

Ground / thermal vias are critical for the proper performance of this device. Vias should use a 0.008 in. diameter drill, and they are solid filled, copper plated shut.

Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1, C2, C3	1.0 µF	Cap, 402, +16V, ±20 %, X5R	Various	–
C4, C5, C6	10.0 µF	Cap, 805, +10 V, ±10 %, X7R	Various	–
R1, R2, R3	0 Ω	Res, 0402, SMT	Various	–
R4, R5, R6	5.1 Ω	Res, 0402, SMT	Various	–

Mechanical Drawing



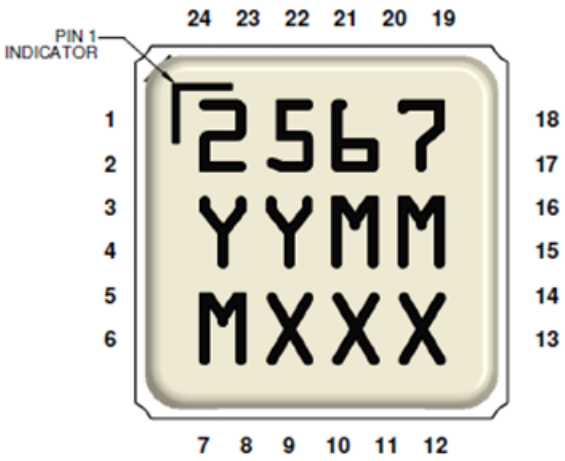
All dimensions are in inches.
Unless specified otherwise, tolerances: ±0.005 in.

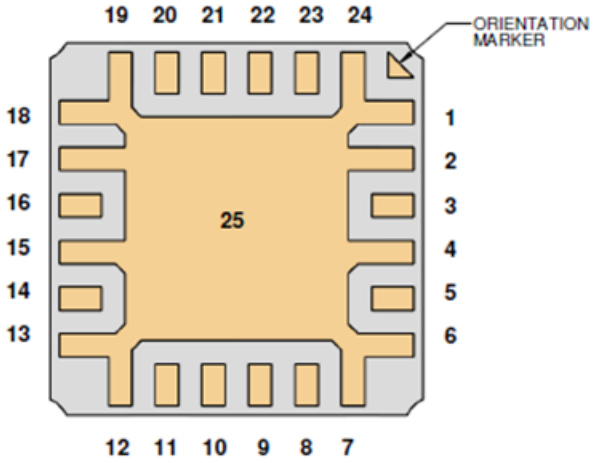
Marking: Part number – 2567
Year/Month code – YYMM
Batch ID – MXXX

Package Materials:
Base Aluminum Nitride (AIN)
Lid Liquid Crystal Polymer (LCP)

Part is EPOXY Sealed
Land Pads are Gold Plated

Pin Layout





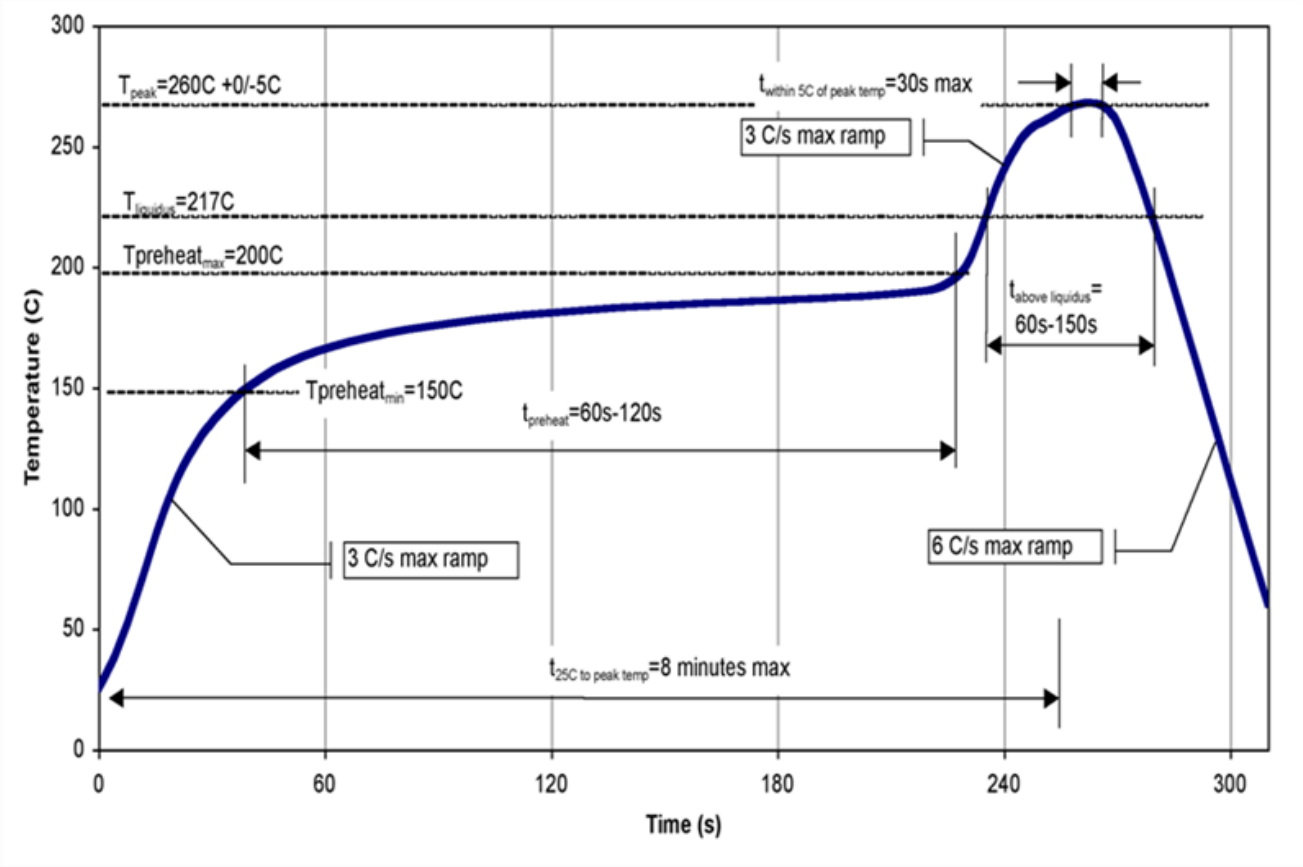
Pad Description

Pin	Symbol	Description
1,2,4,6,7,12,13,15,17-19,24, 25	GND	Backside paddles; must be grounded on PCB. Multiple vias should be employed to minimize inductance and thermal resistance. (2)
3,8-10,14,20,22	N/C	No internal connection; must be grounded on PCB.
5	RF IN	RF input
11	V_{G1}	Gate voltage. Bias network is required. (1)
16	RF OUT	RF output.
21	V_D	Drain voltage. Bias network is required. (1)
23	V_{G2}	Gate voltage. Bias network is required. (1)

Notes:

1. See Application Circuit on page 6 as an example.
2. See Mounting Configuration on page 7 for suggested footprint.

Recommended Soldering Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 0B	ANSI/ESD/JEDEC JS-001
ESD – Charge Device Model (CDM)	Class 3	ANSI/ESD/JEDEC JESD22-C101
MSL – 260 °C Convection Reflow	Level 3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

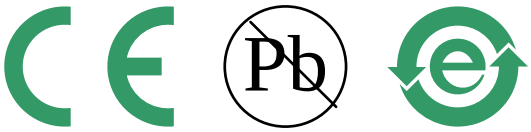
Solderability

Compatible with the latest version of J-STD-020, Lead-free solder, 260 °C

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Lead Free
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free
- Qorvo Green



Contact Information

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