

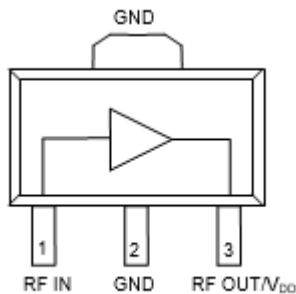
General Description

The TAT7460 is a 75 Ω RF Amplifier that is designed for use up to 2600 MHz, which addresses the CATV and Satellite bands in a single part. The TAT7460 is fabricated using 6-inch GaAs pHEMT technology to optimize performance and cost.



SOT-89 Package

Functional Block Diagram



Key Features

- 50 – 2600 MHz bandwidth
- 2.4 dB Noise Figure <1600 MHz
- Extremely Flat Gain Response
- Low Power Consumption: 100 mA at 5 V

Applications

- CATV Distribution Amplifiers
- Multi-Dwelling Units
- Drop Amplifiers
- Single-ended Gain Blocks
- FTTH Receivers

Ordering Information

Part Number	Description
TAT7460	75 Ω pHEMT Amplifier
TAT7460 EVB	50 – 2600 MHz Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to +150 °C
Device Voltage (V _D)	+10.0 V

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Device Voltage (V _{DD})	4.5	5.0	6.5	V
Device Current (I _{DD})		100	120	mA
Case Temperature	0		+85	°C
T _j for >10 ⁶ MTTF			+150	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

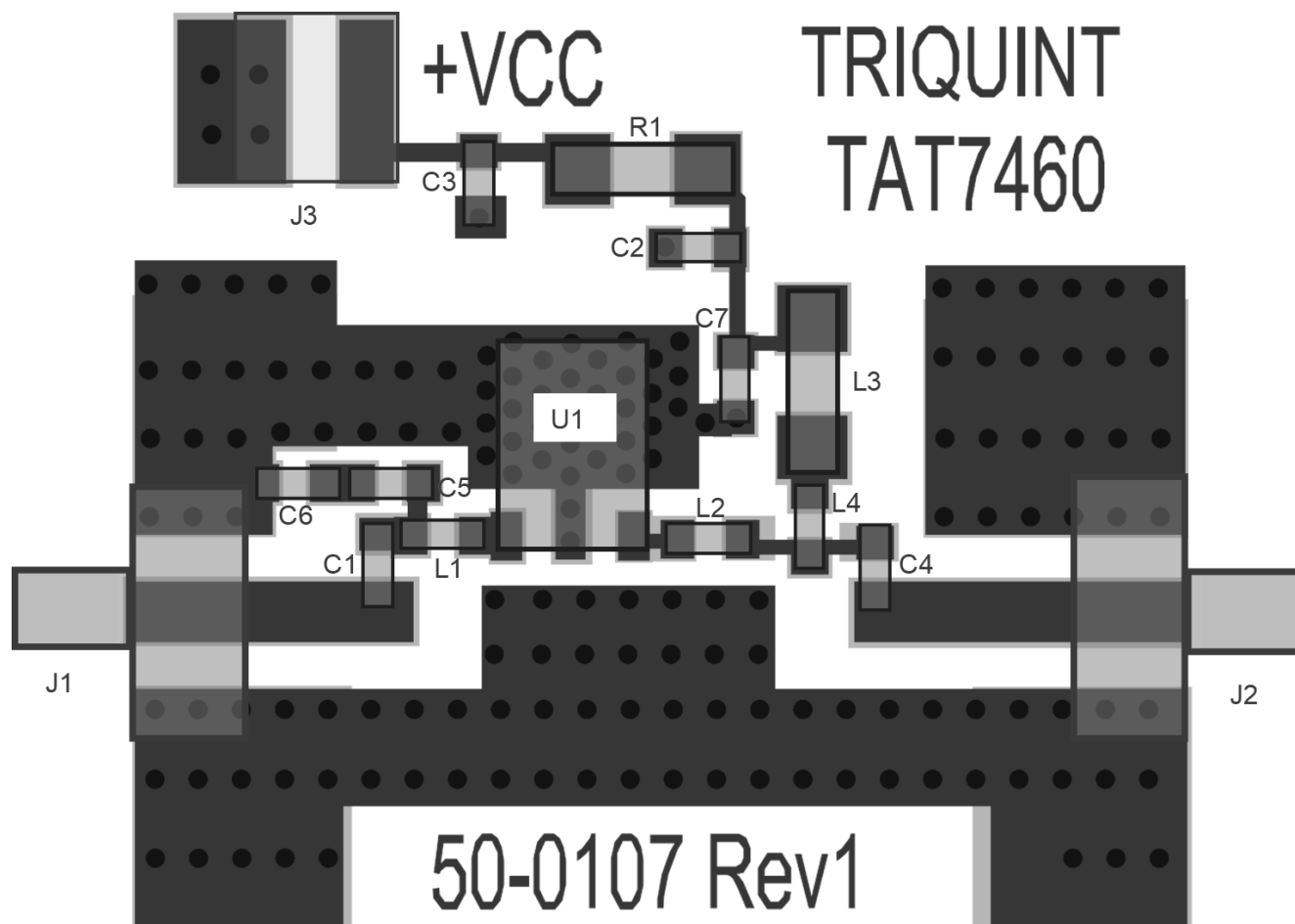
Electrical Specifications

Parameter	Conditions ⁽¹⁾	Min	Typical	Max	Units
Operational Frequency Range		50		2600	MHz
Gain		16.1	16.5		dB
Gain Flatness			+/- 0.5		dB
Input Return Loss			18		dB
Output Return Loss			18		dB
CSO	30 dBmV / channel at output 80 channels flat		-61		dBc
CTB			-72		dBc
XMOD			-71		dBc
Output IP2	P _{out} = +5 dBm / tone Δf = 100 MHz	+56.2	+58		dBm
Output IP3		+31.1	+36		dBm
Output P1dB			+20.5		dBm
Noise Figure	50 – 1600 MHz		2.5		dB
Device Current (I _{DD})			100	120	mA
Thermal Resistance, θ _{jc}	Junction to case		51		°C/W

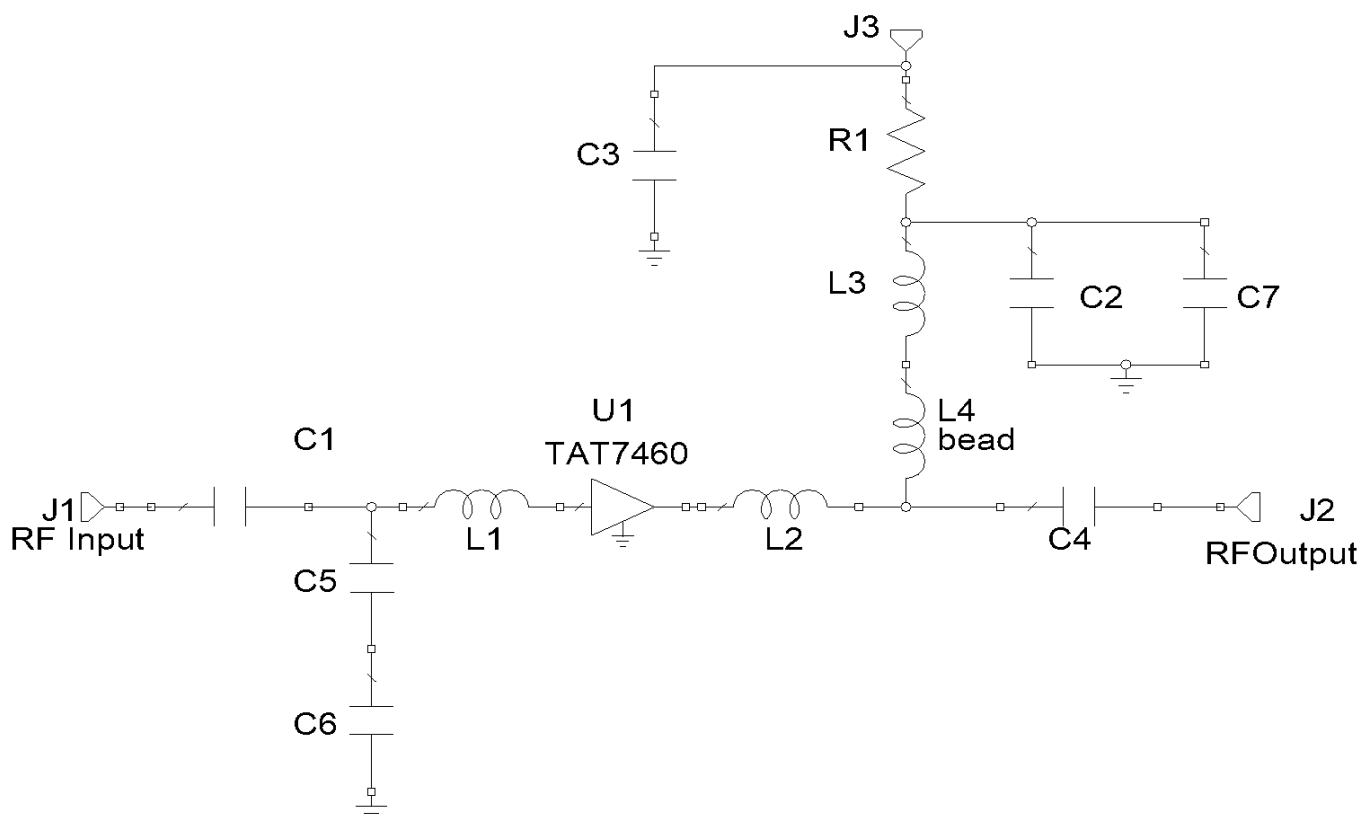
Notes:

1. Test conditions unless otherwise noted: V_{DD} = +5.0 V, Temp = +25 °C, Freq = 50 – 2600 MHz

Evaluation Board Schematic (50 – 2600 MHz)



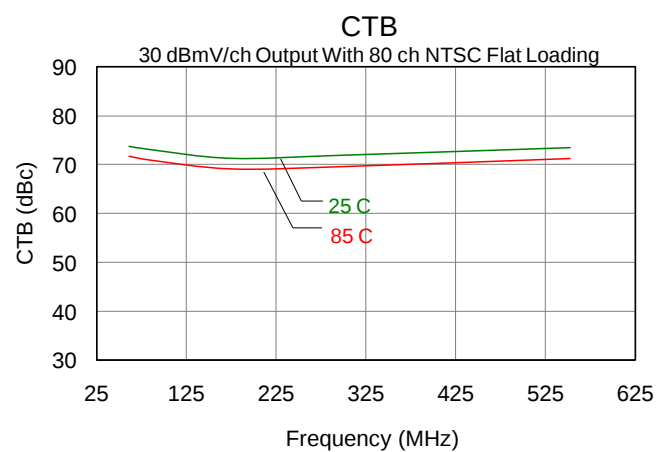
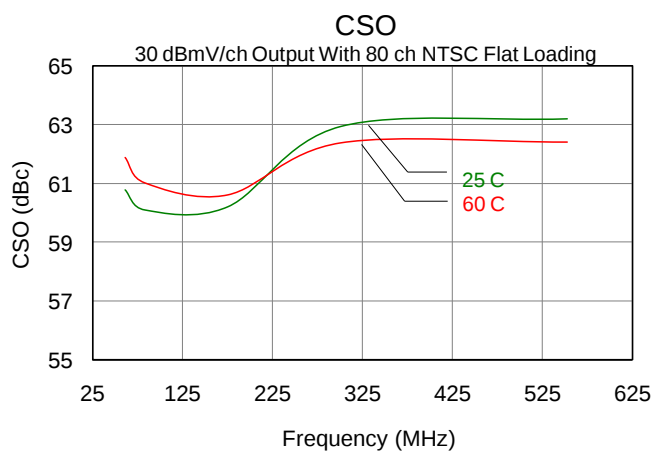
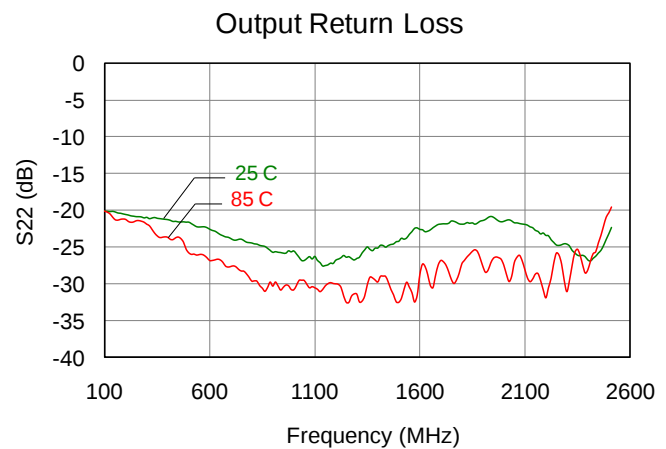
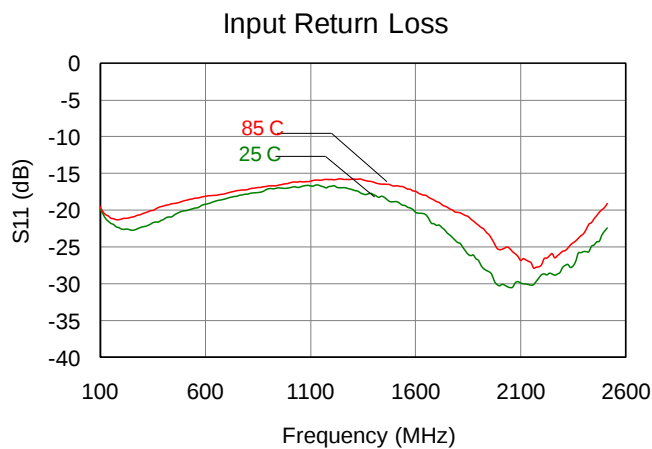
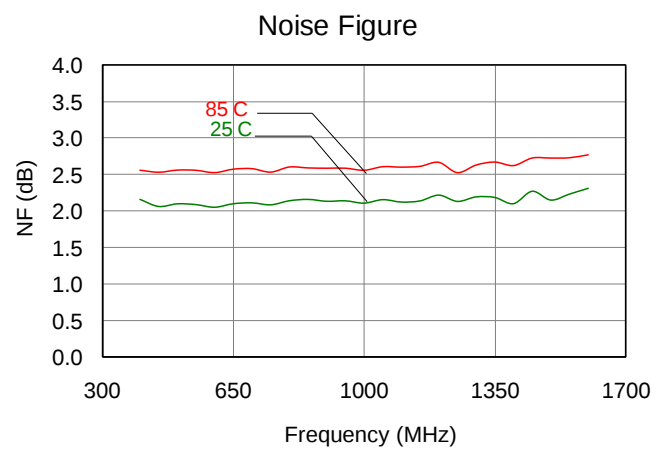
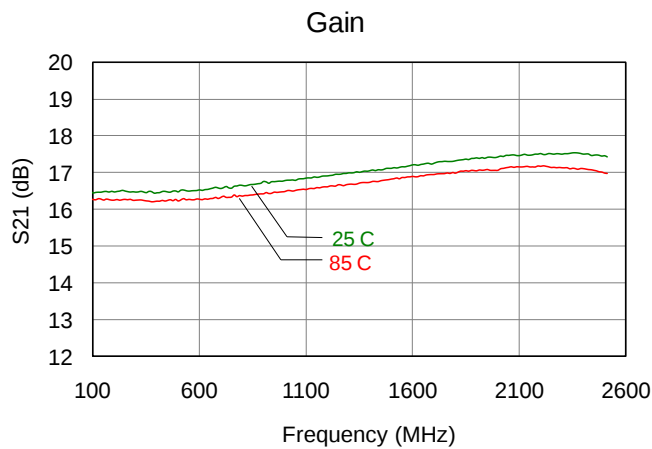
Application Circuit Schematic



Bill of Materials

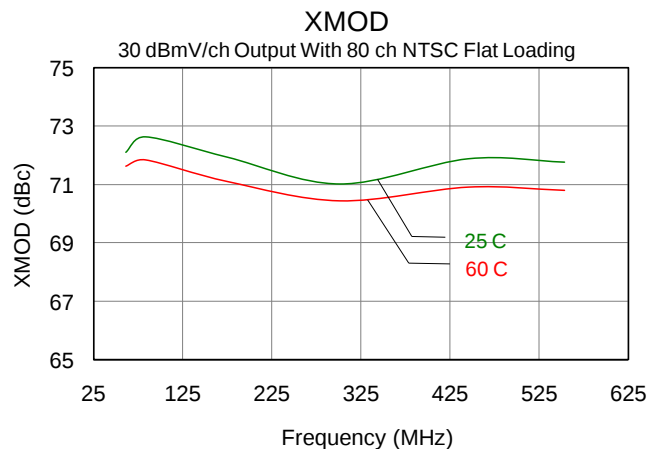
Reference Designator	Value	Description	Manufacturer	Part Number
U1		75 Ω pHEMT Amplifier	Qorvo	TAT7460
C1	470 pF	CAP, 0603, 16V, 5%	Various	
C2, C3, C7	0.01 μF	CAP, 0603, X7R, 16V, 5 %	Various	
C4	390 pF	CAP, 0603, 16V, 5%	Various	
C5	0.7 pF	CAP, 0603, 50V, ±0.1 pF	Various	
C6	0.5 pF	CAP, 0603, 50V, ±0.1 pF	Various	
L1	3.6 nH	IND, 0603, 5%	Coilcraft, Inc	
L2	3.3 nH	IND, 0603, 5%	Coilcraft, Inc	
L3	880 nH	IND, 1206, 5%	Gowanda	
L4	Bead	Ferrite Bead, 0402, 200mA, 1.0 kΩ	Murata	BLM15AG102SN1
R1	0 Ω	RES, 1206	Panasonic	
J1, J2	Connector	F-Connector	Millimeter Wave	

Performance Plots

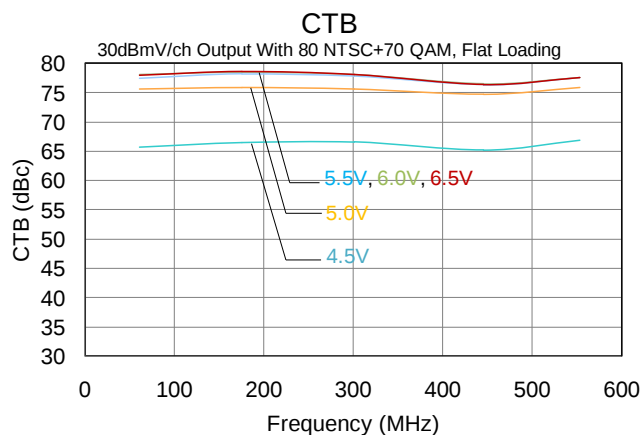
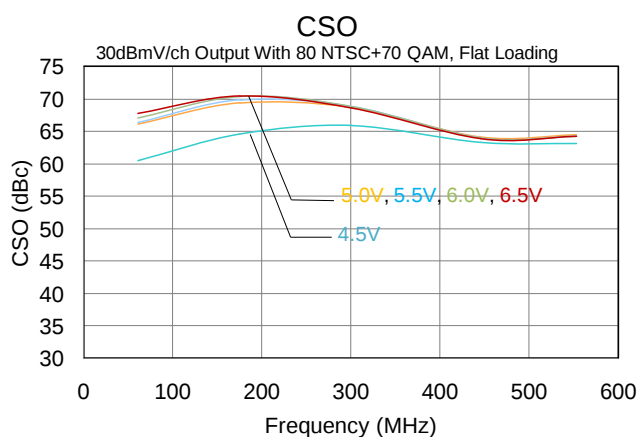
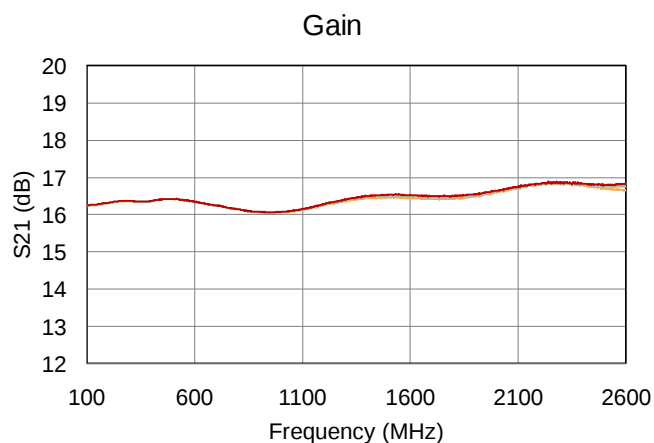
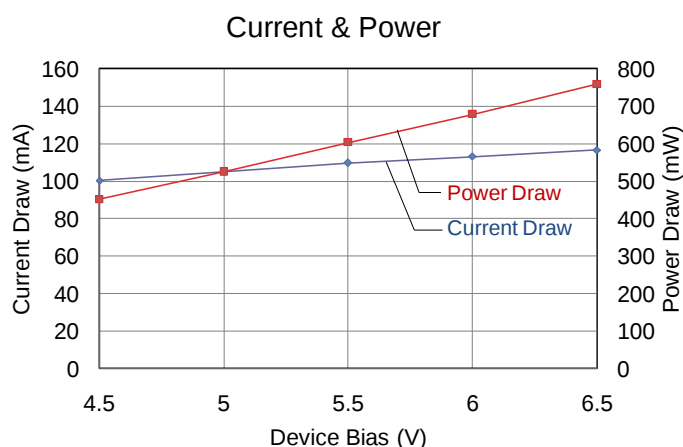


Test conditions unless otherwise noted: $V_{DD} = +5V$, $I_{DD} = 100mA$, Temp = +25°C

Performance Plots (Cont'd)

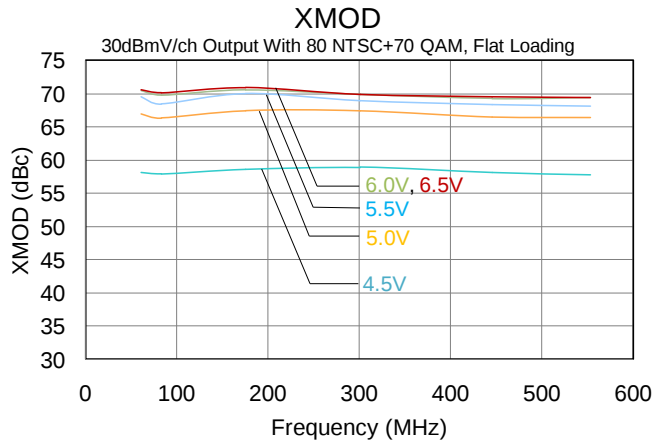
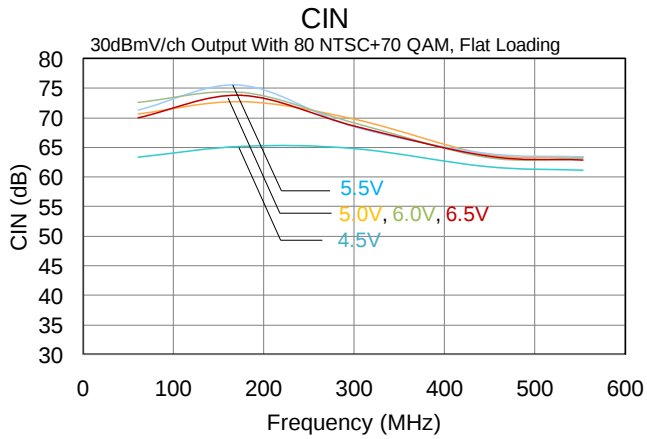


Performance Plots Over Bias



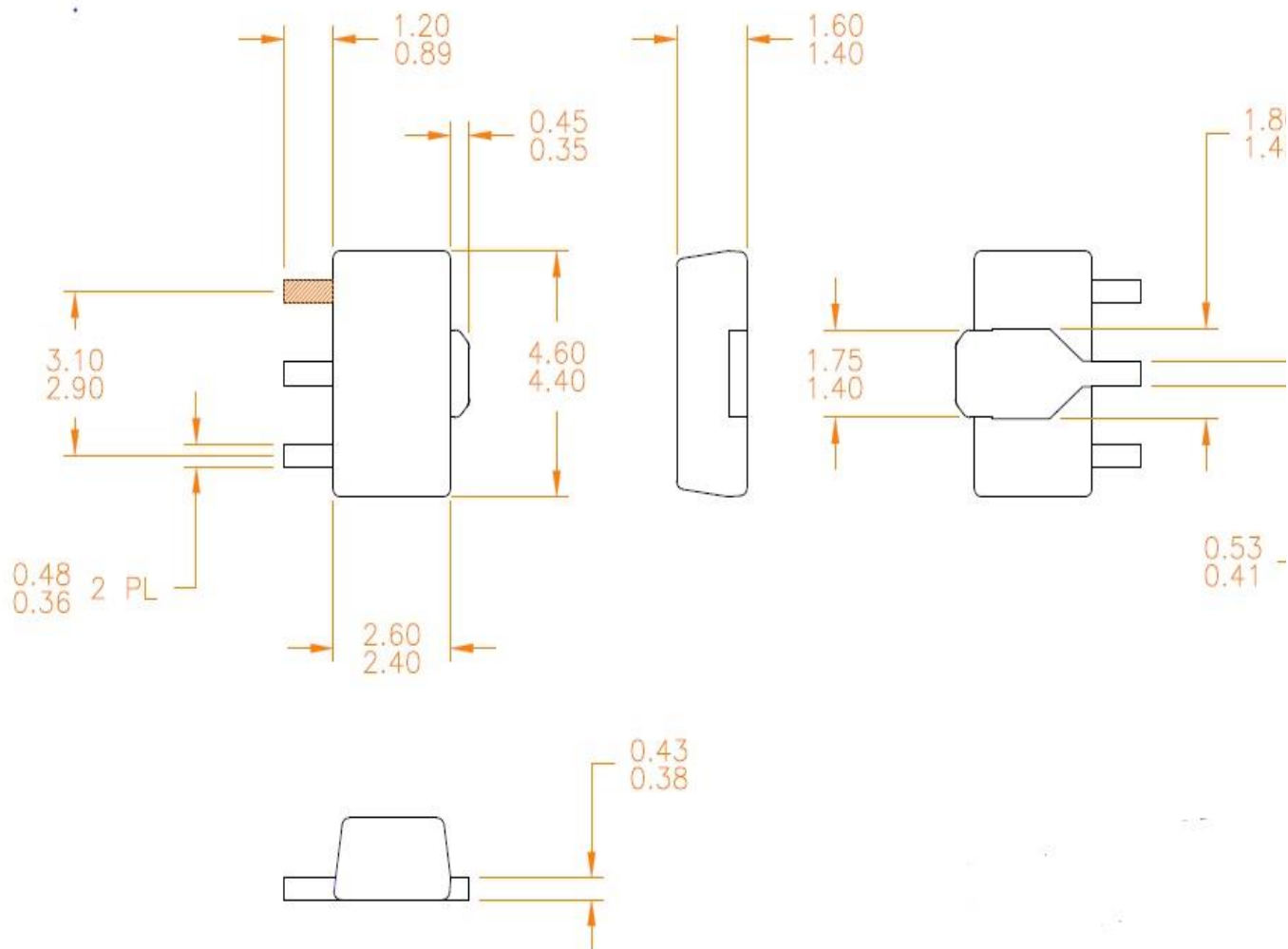
Test conditions unless otherwise noted: $V_{DD} = +4.5$ to 6.5 V, $I_{DD} = 100 - 120$ mA, Temp = $+25^{\circ}\text{C}$

Performance Plots Over Bias (cont'd)

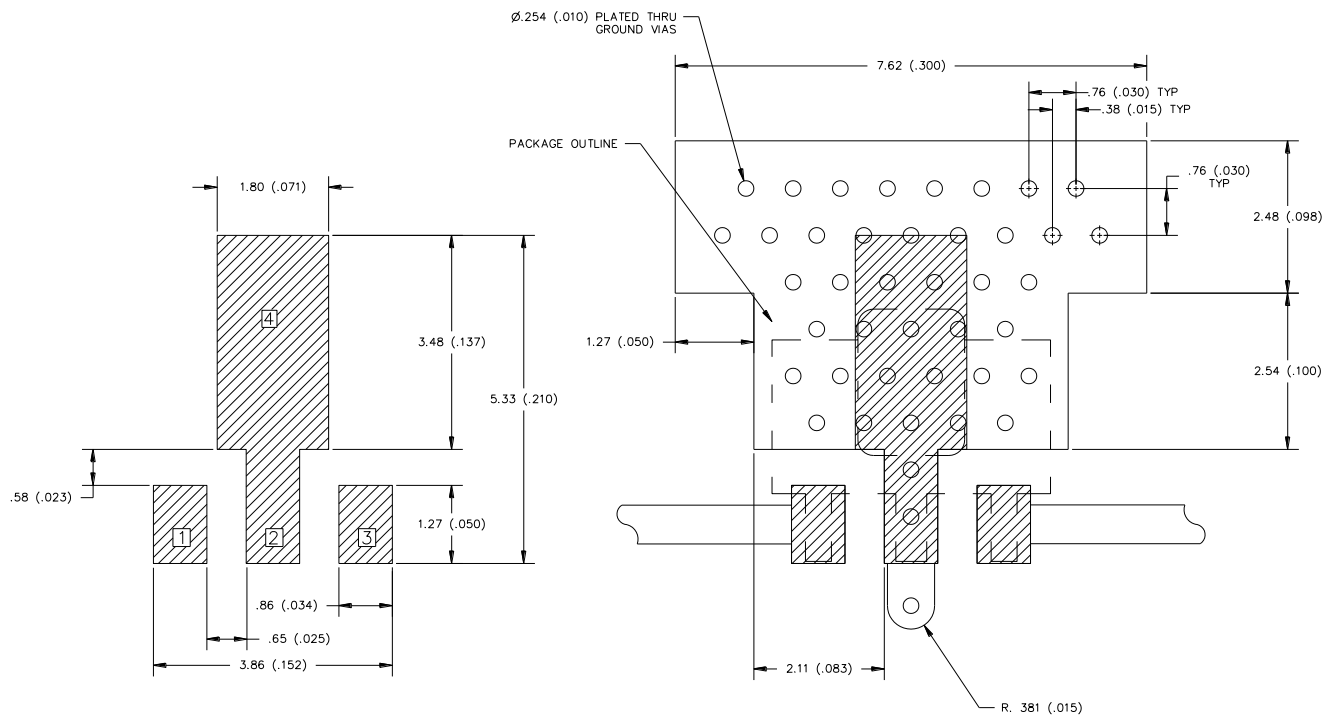


Test conditions unless otherwise noted: $V_{DD} = +4.5$ to 6.5 V, $I_{DD} = 100 - 120$ mA, Temp = $+25^{\circ}\text{C}$

Package Marking and Dimensions



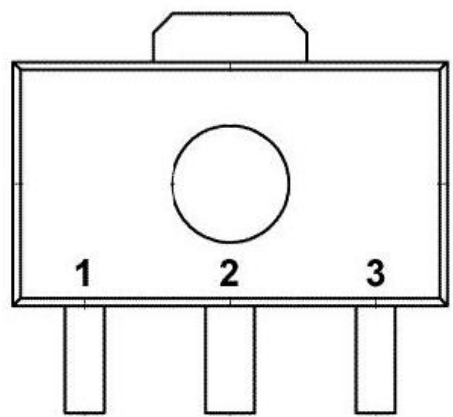
PCB Mounting Pattern



Notes:

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35 mm (#80/.0135") diameter drill and have a final, plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. RF trace width depends upon the PC board material and construction.

Pin Configuration and Description



Pin Number	Label	Description
1	RF IN	RF input pin. DC blocking capacitor required.
2	GND	Ground connection.
3	RF OUT	RF output and bias pin. VDD bias choke required.
Backside Paddle	GND	Ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1A+	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class IV	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260 °C max. reflow temp.) soldering process.

Solder profiles available upon request.

Contact plating: Matte Sn

RoHS Compliance

This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free
- Qorvo Green



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Email: customer.support@qorvo.com

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