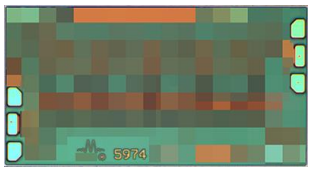
BROADBAND DISTRIBUTED AMPLIFIER ADM-5974CH

The ADM-5974CH is a broadband, moisture resistant MMIC LO buffer amplifier. The ADM-5974 provides efficient, optimized LO drive to all Marki mixers in band with no required negative bias or sequencing. It is built with a moisture resistant pHEMT process to allow the bare chip to pass biased HAST testing without a hermetic seal. Second harmonic rejection can be tuned to very low levels using the optional negative bias. The ADM-5974 can also be used as a broadband signal amplifier. The bare die features enhanced moisture resistance for improved reliability.



Bare Die

Features

- Optimized for use as a T3 LO buffer amplifier
- Fast <10 ps risetime
- 3rd and 5th Harmonic Generation
- Broadband 50 Ω Matching
- Unconditionally Stable
- Enhanced Moisture Resistance

Electrical Specifications - Specifications measured in a 50-Ohm system.

Parameter	Frequency (GHz)	Typ
Saturated Output Power with negative bias (dBm)	DC to 35	+22
Output 1 dB Compression (dBm)		+20
Small Signal Gain with negative bias (dB)		14
Return Loss (dB)		16
Phase Noise (10 kHz Offset) (dBc/Hz)		-153
Noise Figure (dB)		6
Third Order Output Intercept Point (dBm)		27
Bias Requirements, External (mA)		
Vd: +5.0 to +7.0 / Vg: -0.25 Volts		150
Vd: +5.0 to +7.0 / Vg: 0 Volts		220

Part Number Options

Model Number	Description	Green Status	Product Lifecycle	Export Classification
ADM-5974CH	Chip	RoHS	Active	EAR99
ADM-5974S	TBA			
ADM-0026-5929SM[1]	Surface Mount 4mm QFN			
EVAL-ADM-5929SM[1]	EVAL Board			
ADM1-0026PA[1]	Connectorized Module (with Bias Tee)			

[1] Note: Datasheets for other package options are available on the Marki Microwave website

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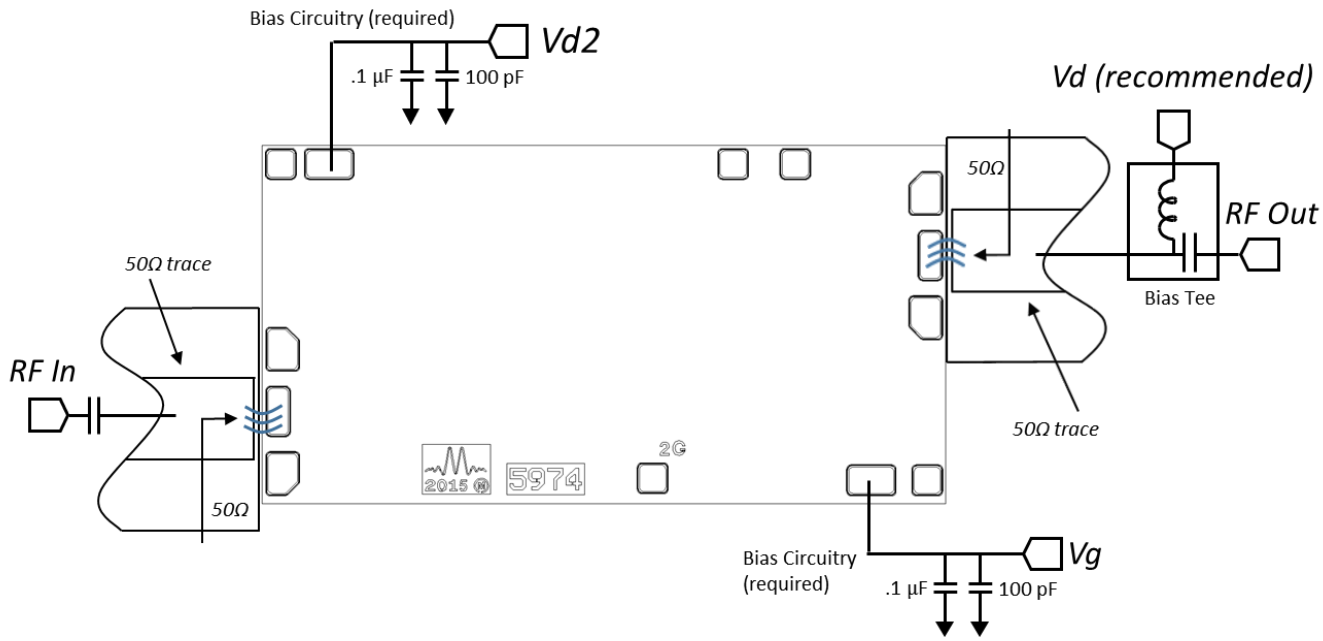
Frequency DC to 35 GHz

Functional Diagram and Application Circuit



Biasing and Operation

RF In / RF Out – Input and output signals should be connected by 50 ohm microstrip or coplanar traces to well matched 50 ohm sources and loads. DC blocking capacitors and bias tees are required.

Vg – Negative gate voltage is optional to improve lifetime of the amplifier and reduce current consumption. Harmonic generation is also significantly affected by the negative gate voltage level. It may be supplied through the Vg pad or through the RF input pad using an external bias tee

Vd- It is recommended that bias voltage Vd is applied through a bias tee on the RF output, but bias supply can also be supplied to Vd through Vd2 pad if desired. This will result in increased operating temperature and slightly reduced gain and power output. Bias supply should be voltage limited below 9 V and current limited below 250 mA at all times. The operational bias voltage should be between 3 V and 7 V for full small-signal gain, or between 5 V and 7 V for full gain, linearity and power output. If bias tee on RF output is used, pad Vd2 voltage should be left unconnected (*not* grounded).

Bias Circuitry – The capacitors on the Vd and Vg lines prevent low frequency oscillation. They may be reduced or omitted in bias circuits with sufficient low-frequency loss. Designers are encouraged to experiment if they want to modify or omit the bias circuitry.

DC/RF Ground – The back of the chip should be connected to a low noise RF and DC ground with very low electrical and thermal resistance for high frequency operation and thermal heat sinking.

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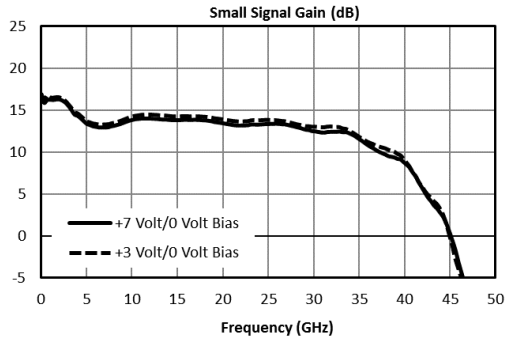
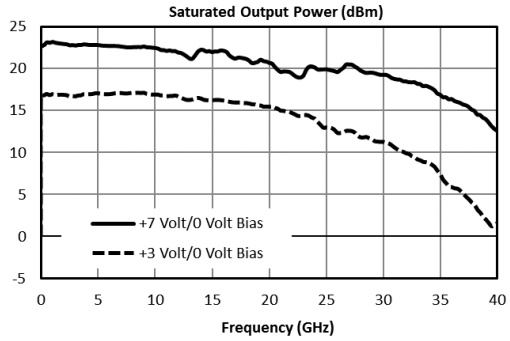
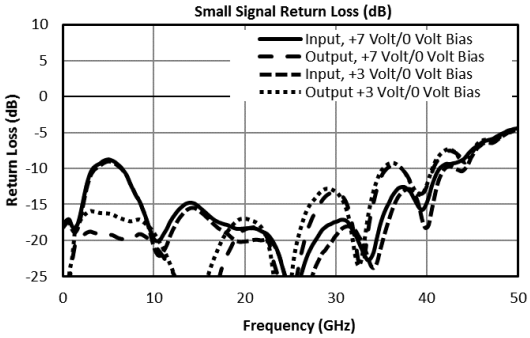
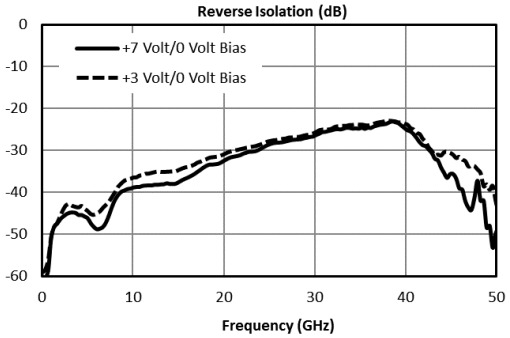
Frequency DC to 35 GHz

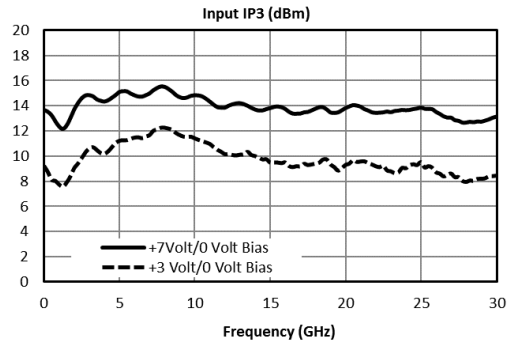
Typical Performance: Positive Only (+3, +7V) Bias (Bias tee on RF output), Grounded Gate (Bias tee on RF input)

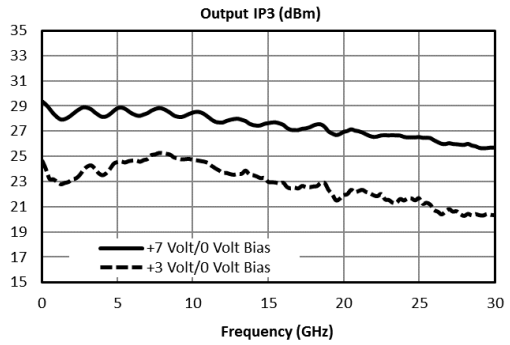


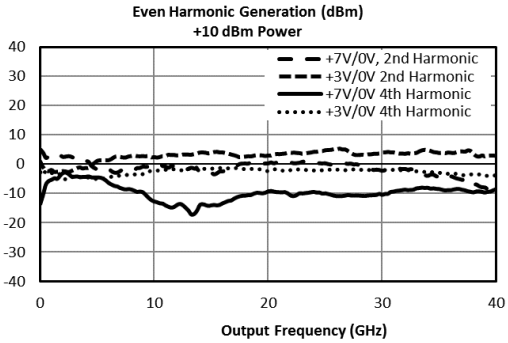


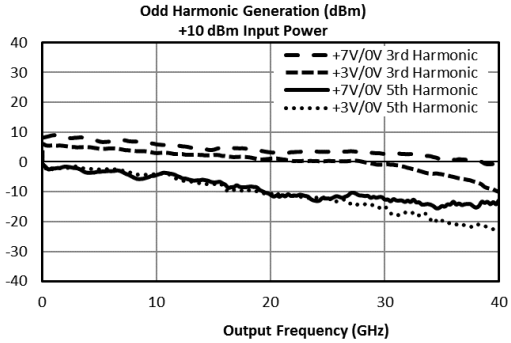




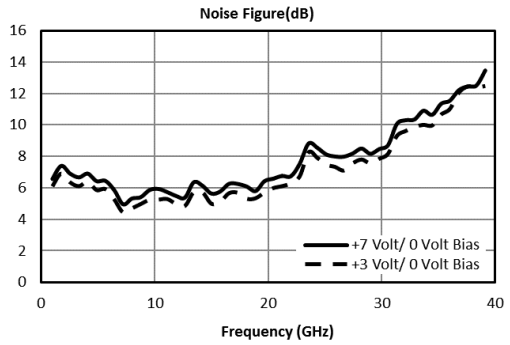


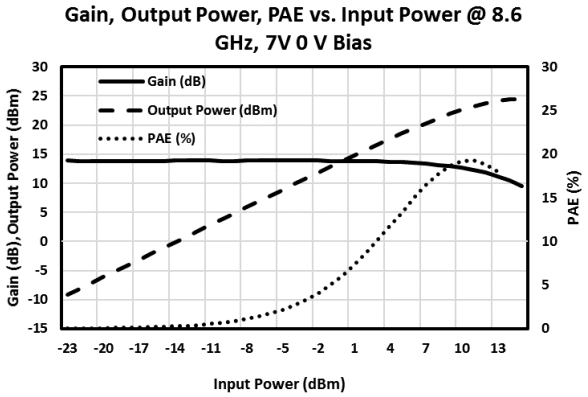


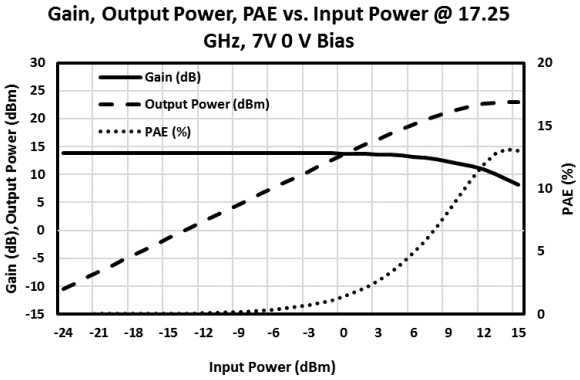


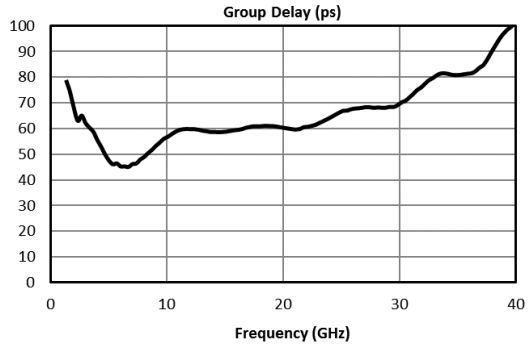


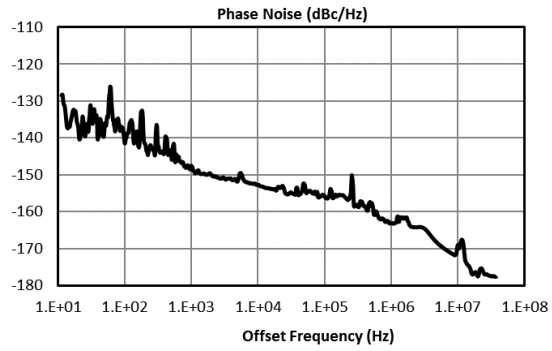
Typical Performance: Positive Only (+3, +7V) Bias, Grounded Gate (Continued)

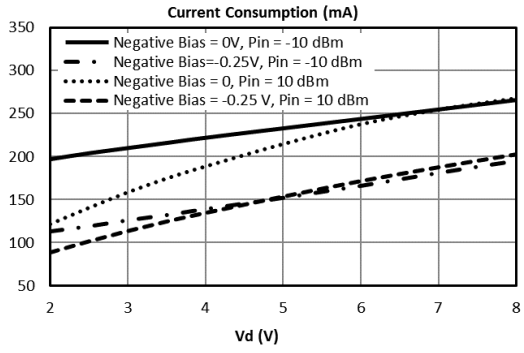




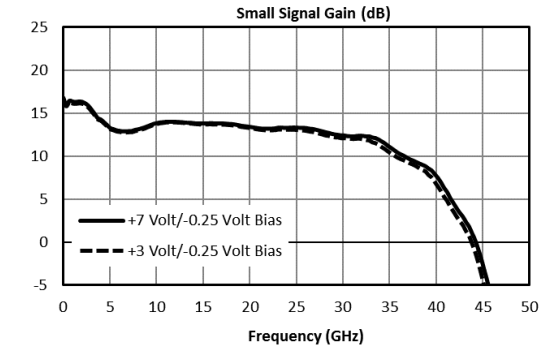


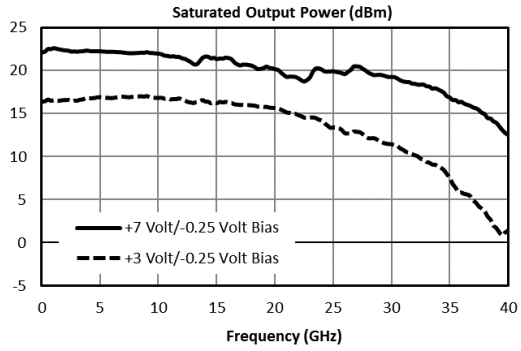


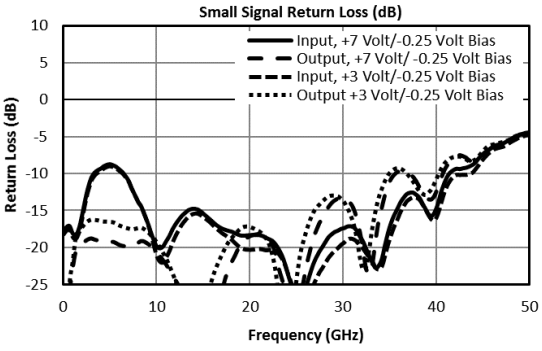


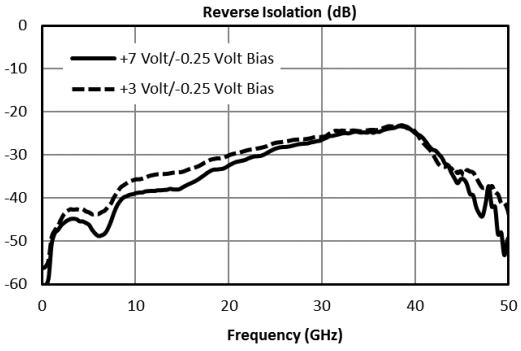


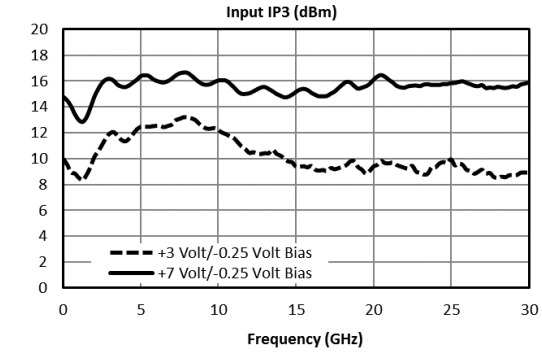
Typical Performance: +3, +7V Positive Bias, -0.25 Negative Bias

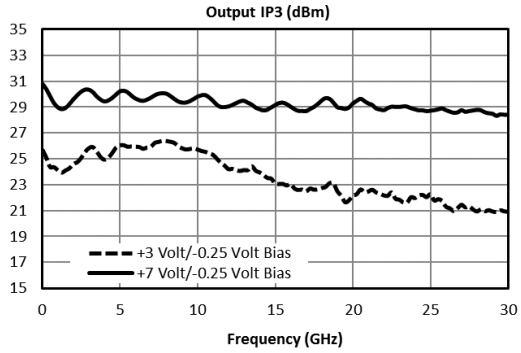




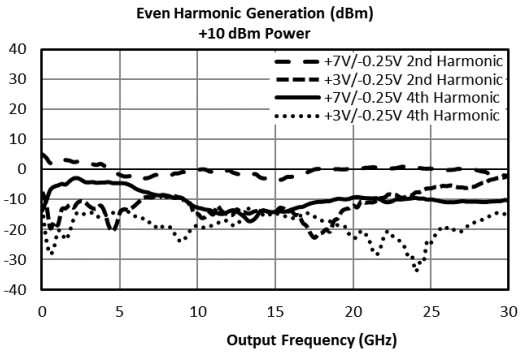


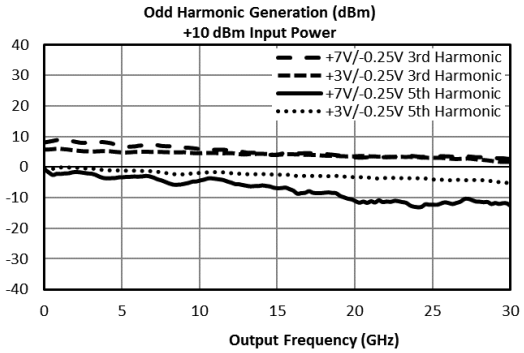


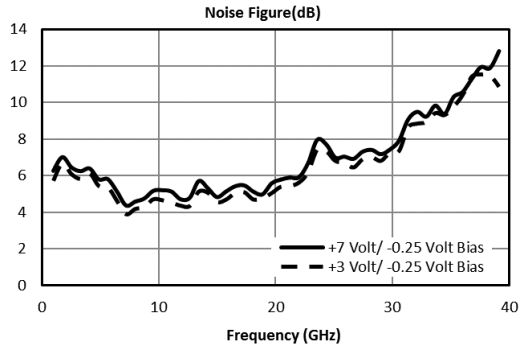


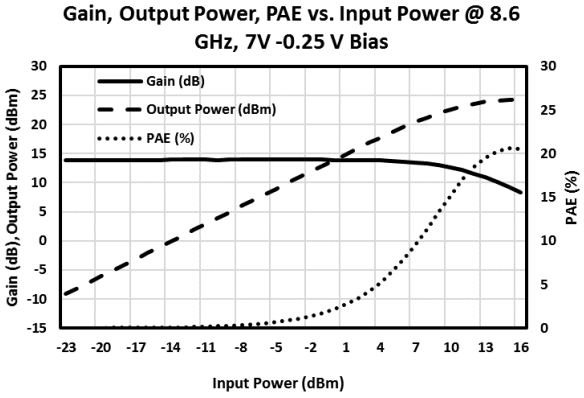


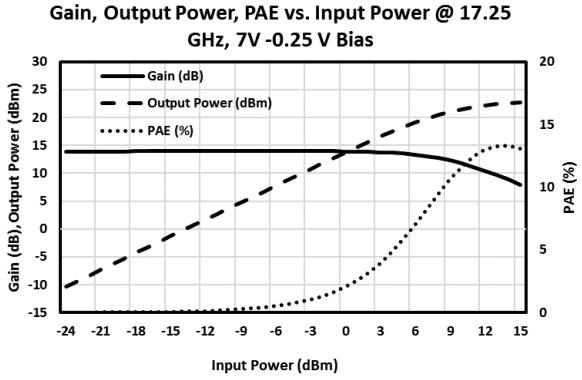
Typical Performance: +3, +7V Positive Bias, -0.25 Negative Bias (Continued)



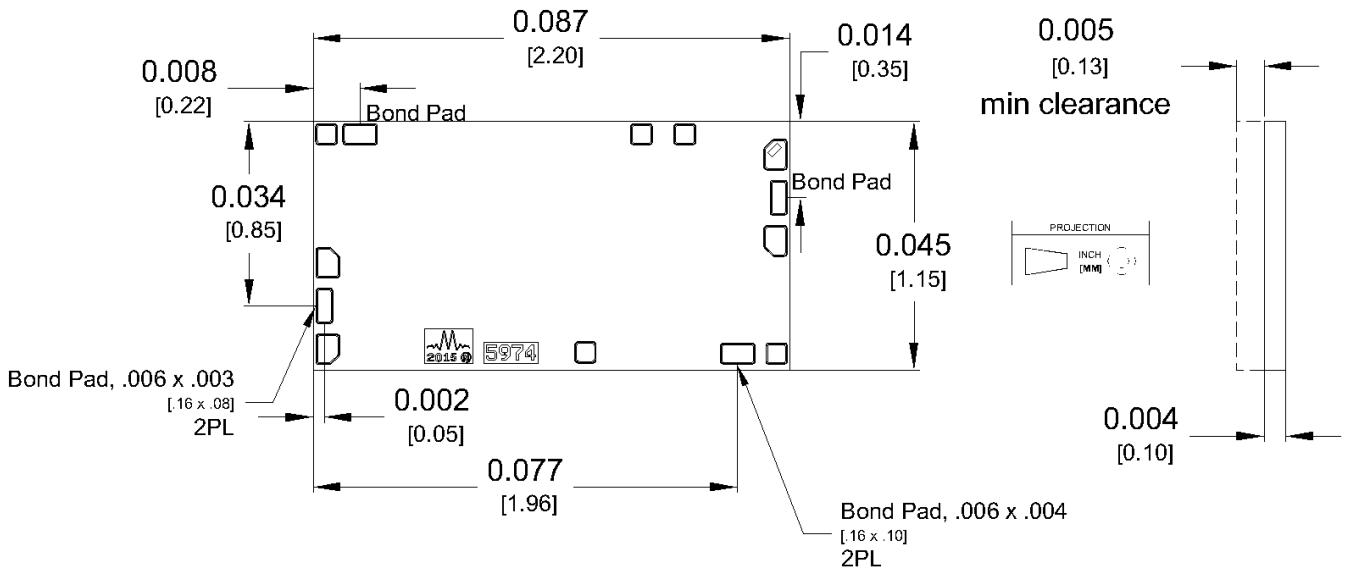






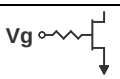


Chip Outline Drawing



RF GSG probe pitch is 200 µm

All unlabeled pads are ground pads

Port Descriptions		
Function	**Description**	**Interface Schematic**
RF in	This pin is DC coupled and matched to 50 Ω.	
Vg	Gate control for the amplifier. External decoupling capacitors are required.	
RF out / Vd	This pad is DC coupled and matched to 50 Ω.	
Vd2	Optional drain bias port. External decoupling capacitors are required.	
GND	Back of chip should be connected to RF/DC ground with low electrical and thermal resistance.	

Absolute Maximum Ratings	
Parameter	**Maximum Rating**
Positive Bias Voltage	9 V
Positive Bias Current	275 mA
Negative Bias Voltage	-2 V
Negative Bias Current	2 mA
RF Input Power	+20 dBm
Power Dissipation	2 W
Thermal Resistance, θ_{jc}	0.873 C/W
ESD (Human Body Model)	Class 0
Operating Temperature	-55ºC to +85ºC
Storage Temperature	-65ºC to +150ºC

DATA SHEET NOTES:

1. Specifications are subject to change without notice. Contact Marki Microwave for the most recent specifications and data sheets.

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