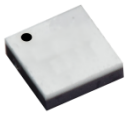
BROADBAND DISTRIBUTED AMPLIFIER ADM-0012-5931SM

The ADM-0012-5931SM is a small, low power, and economical T3 driver or T3A pre-amplifier. It is a GaAs PHEMT distributed amplifier in a 3mm QFN surface mount package. The ADM-0012-5931SM can provide LO drive for 'L', 'M', 'I', and 'H' level mixers, with 11.5 dB typical gain and +19 dBm typical saturated output power for only 85 mA of current. The amplifier can be biased with internal circuitry, or with an external bias network for lower voltage and single supply operation. Additional applications include amplification of clock signals and other general purpose driver applications in electronic warfare and test and measurement.



Features

- Optimized for use as a T3 LO buffer amplifier
- 3rd and 5th Harmonic Generation
- Suitable for driving L, M, and I diode mixers
- Optional Positive Only Bias or Internal Bias Operation
- Broadband 50 Ω Matching
- Unconditionally Stable

Electrical Specifications - Specifications measured in a 50-Ohm system.

Parameter	Frequency (GHz)	Min	Typ	Max
Input for Saturated Output (dBm)	DC to 12.0	+5	+10	+12
Output 1 dB Compression (dBm)			+16	
Saturated Output Power with negative bias (dBm)			+19	
Small Signal Gain with negative bias (dB)			11.5	
Input Return Loss (dB)			13	
Output Return Loss (dB)			14	
Noise Figure (dB)			4.5	
Third Order Output Intercept Point (dBm)			26	
Bias Requirements, Internal (mA) Vd: +10.0 to +12.0 / Vg:-0.25 Volts			85	
Bias Requirements, External (mA) Vd: +5.0 to +7.0 / Vg: -0.25 Volts Vd: +5.0 to +7.0 / Vg: 0 Volts			85 115	

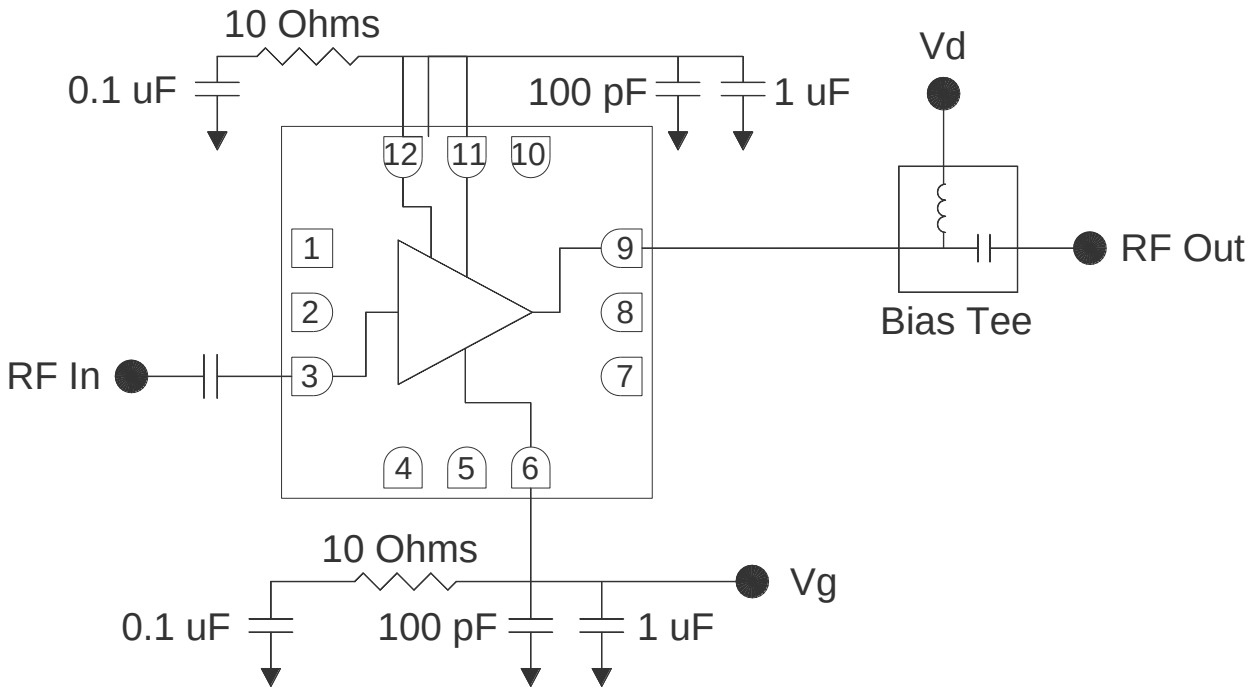
Part Number Options

Model Number	Description
ADM-0012-5931SM [1]	Surface Mount 3mm QFN
EVAL3-ADM-5931	Connectorized Evaluation Fixture

[1] Note: For port locations and I/O designations, refer to the drawings on pages 2, 8, 11, and 12 of this document.

GaAs MMIC devices are susceptible to Electrostatic Discharge. Use proper ESD precautions when handling these items.

Functional Diagram and Application Circuit – External Positive Bias (Pin 9 Output with Bias Tee)



Biasing and Operation

RF In / RF Out – Input and output signals should be connected by 50 ohm microstrip or coplanar traces to well matched 50 ohm sources and loads. DC blocking capacitors or bias tees are required.

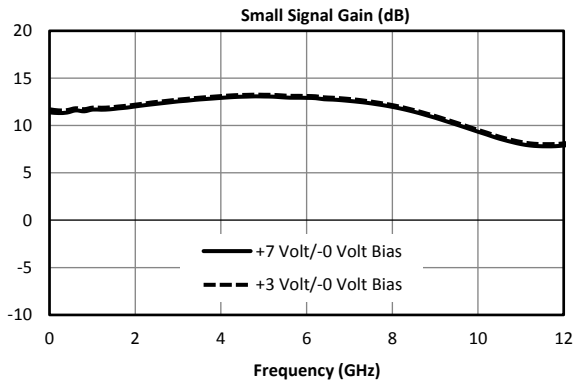
Vg – Negative gate voltage is optional to improve lifetime of the amplifier and reduce current consumption. Harmonic generation is also significantly affected by the negative gate voltage level. The amplifier is designed for optimal performance when the negative gate voltage is tuned such that the *positive* bias supply is 85 mA. It may be supplied through pin 6 or through the RF input on pin 3.

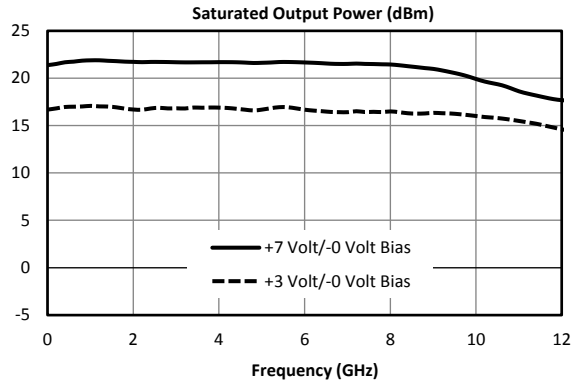
Vd- Bias supply supplied to Vd through pin 9 should be voltage limited below 9 V and current limited below 150 mA at all times. The operational bias voltage should be between 3 V and 7 V for full gain, efficiency, and linearity. In general gain, linearity, and output power will increase marginally with increased voltage from 5 to 7 V.

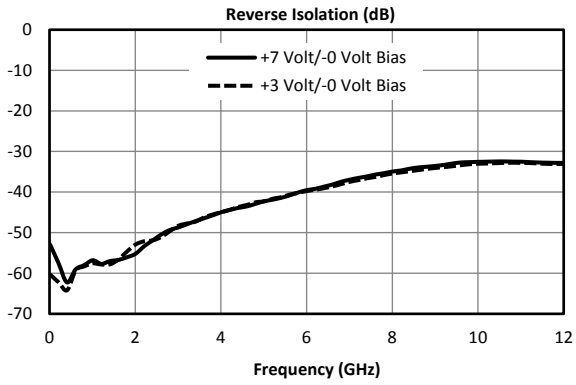
Optional Bias Circuitry – The resistor and capacitor on the Vd and Vg lines (pads 11, 12, and 6) prevent low frequency oscillation. These components are not required in bias circuits with sufficient low frequency loss. Designers should experiment to determine if they are necessary.

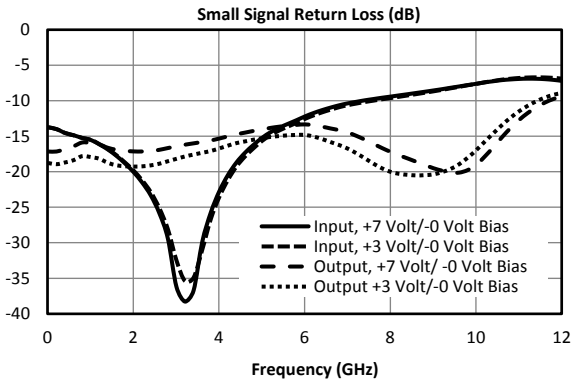
DC/RF Ground – The ground paddle of the QFN should be connected to a low noise RF and DC ground with very low electrical and thermal resistance for high frequency operation and thermal heat sinking.

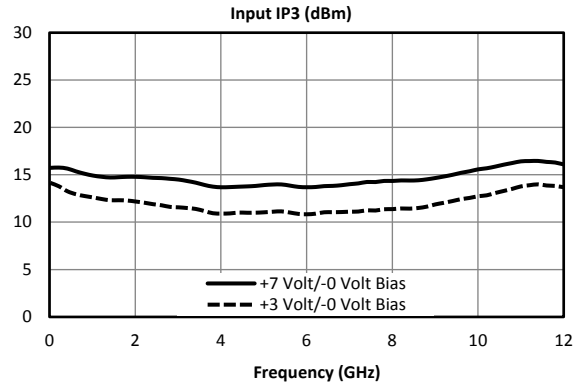
Typical Performance – Positive Only (+3 to +7V) External Bias (Pin 9 Output), Grounded Gate (Pin 6)

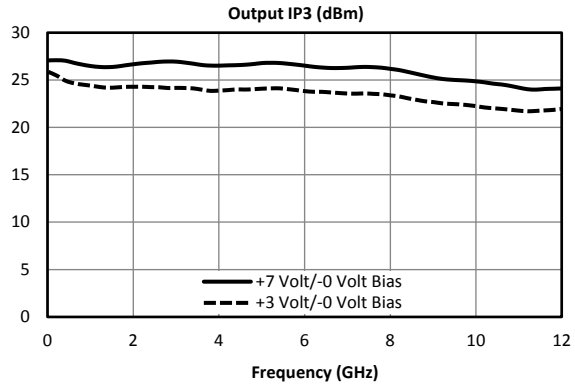




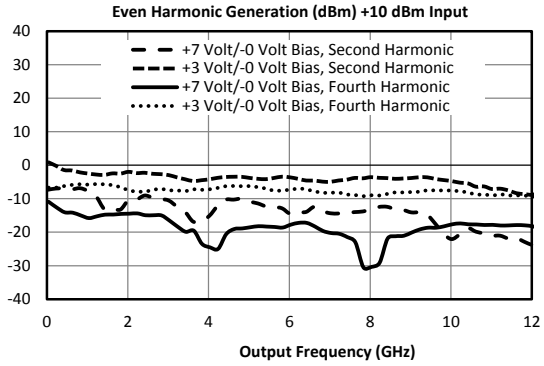


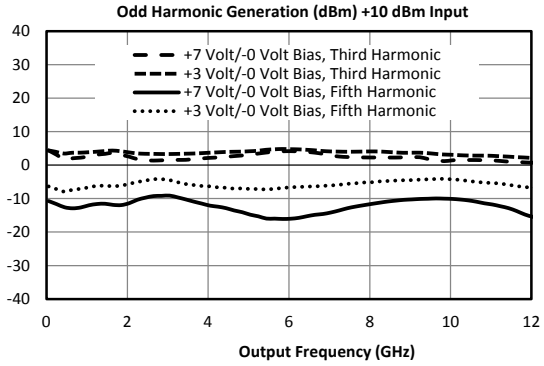


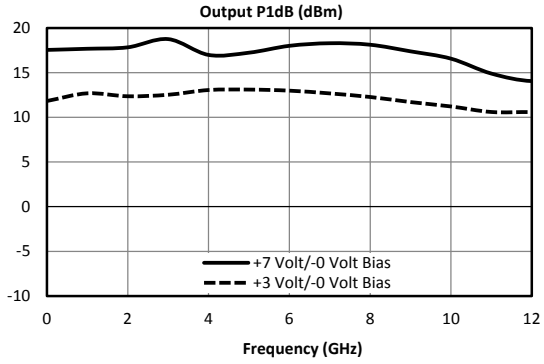


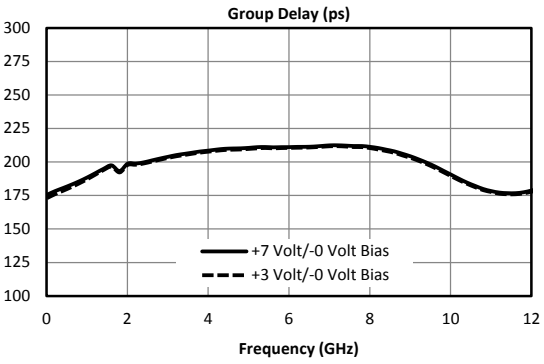


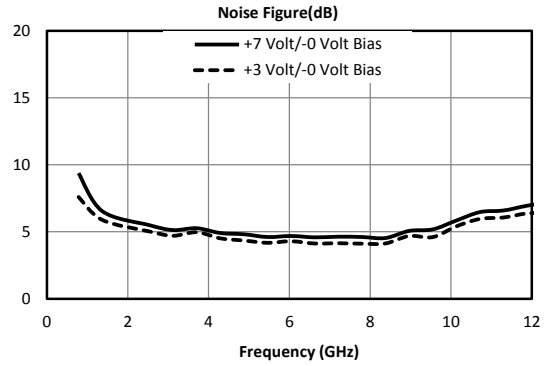
Typical Performance – Positive Only (+3 to +7V) External Bias (Pin 9 Output), Grounded Gate (Pin 6), continued

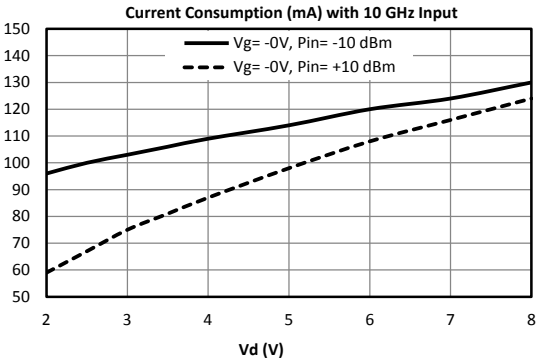




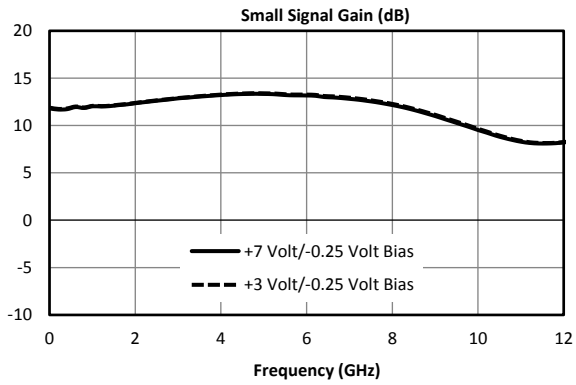


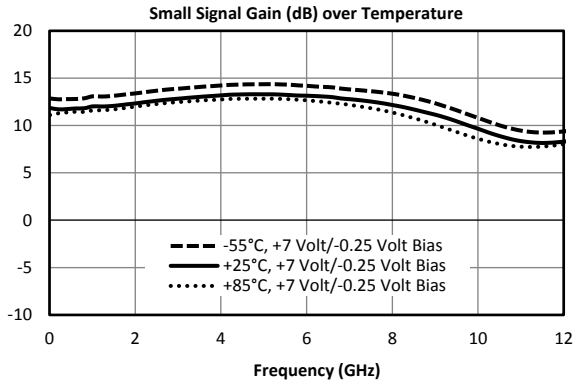


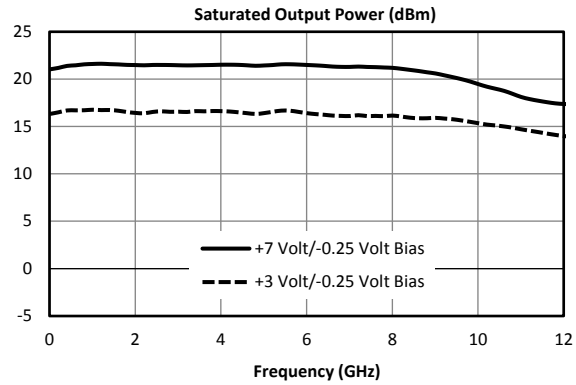


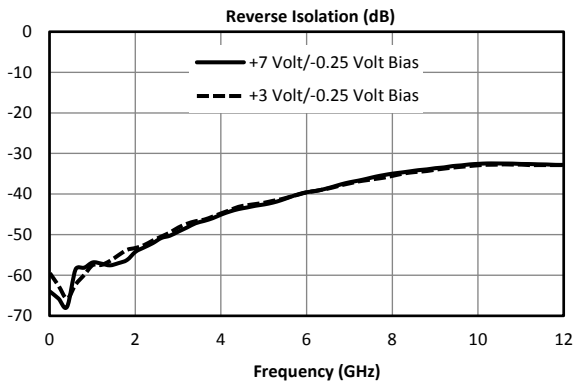


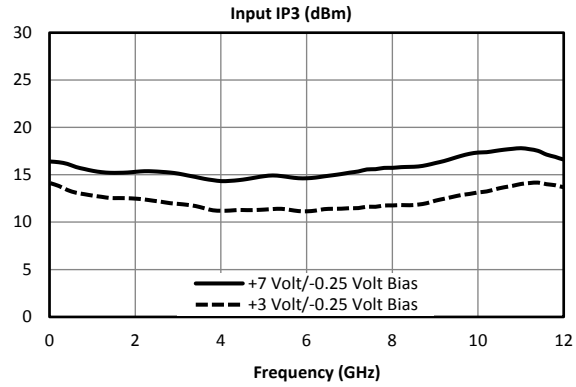
Typical Performance – +3 to +7V External Bias (Pin 9 Output), -0.25 Negative Bias (Pin 6)

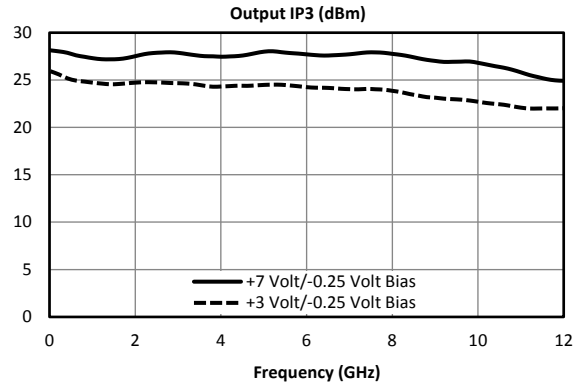




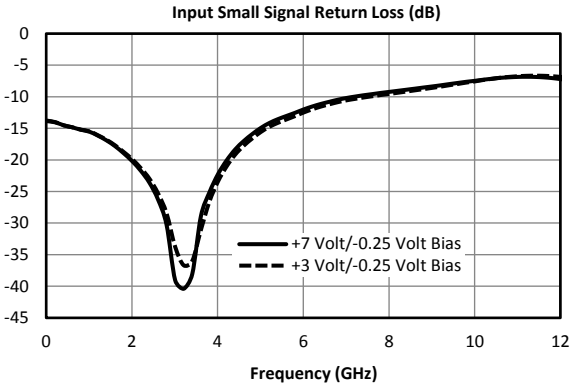


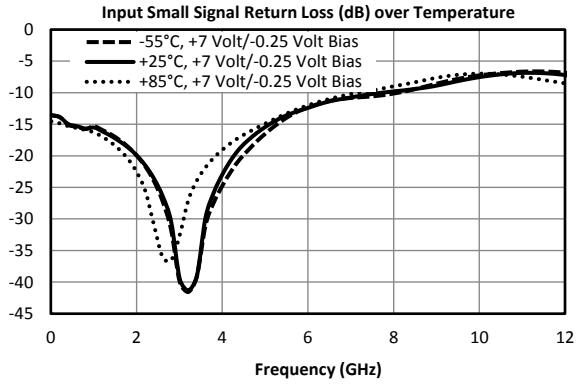


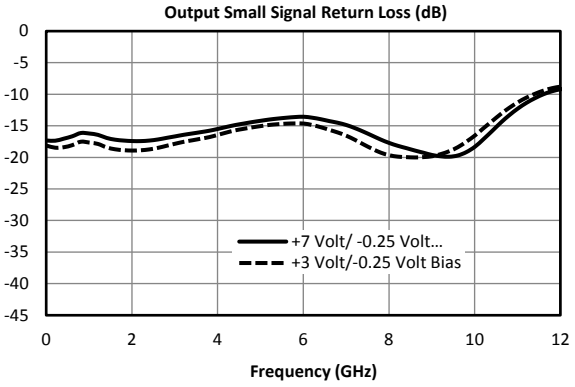


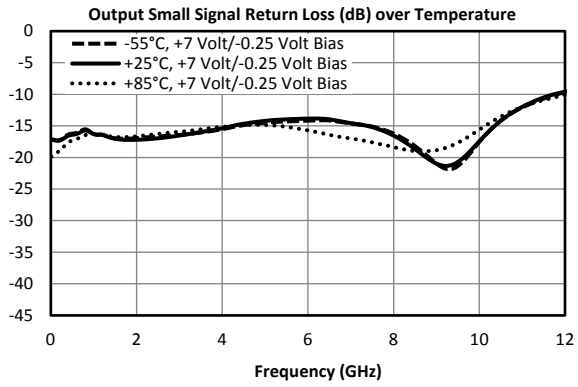


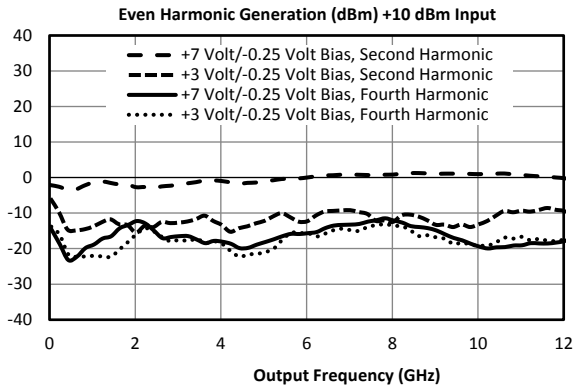
Typical Performance – +3 to +7V External Bias (Pin 9 Output), -0.25 Negative Bias (Pin 6) continued

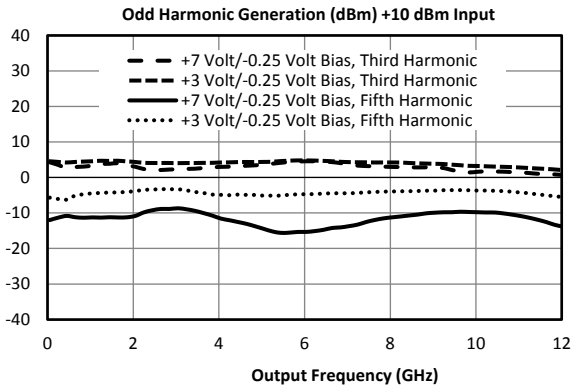




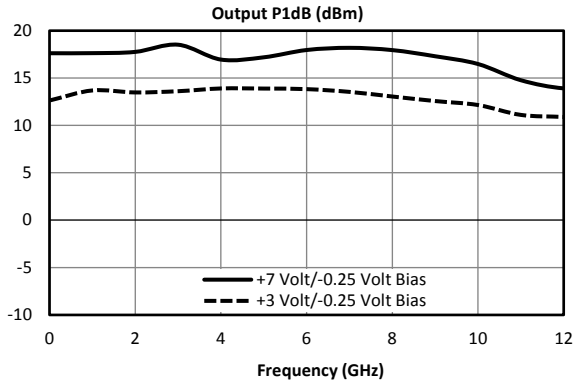


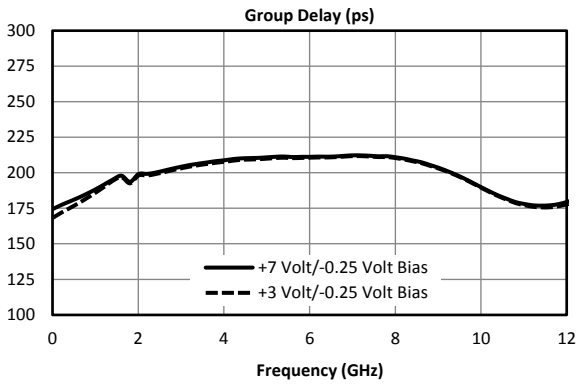


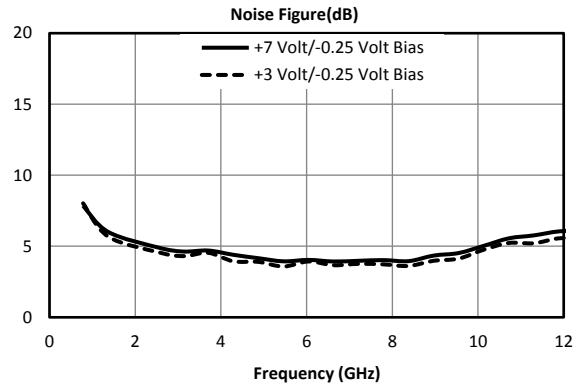


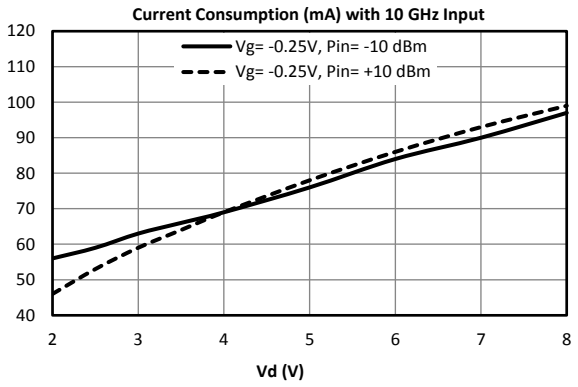


Typical Performance – +3 to +7V External Bias (Pin 9 Output), -0.25 Negative Bias (Pin 6) continued

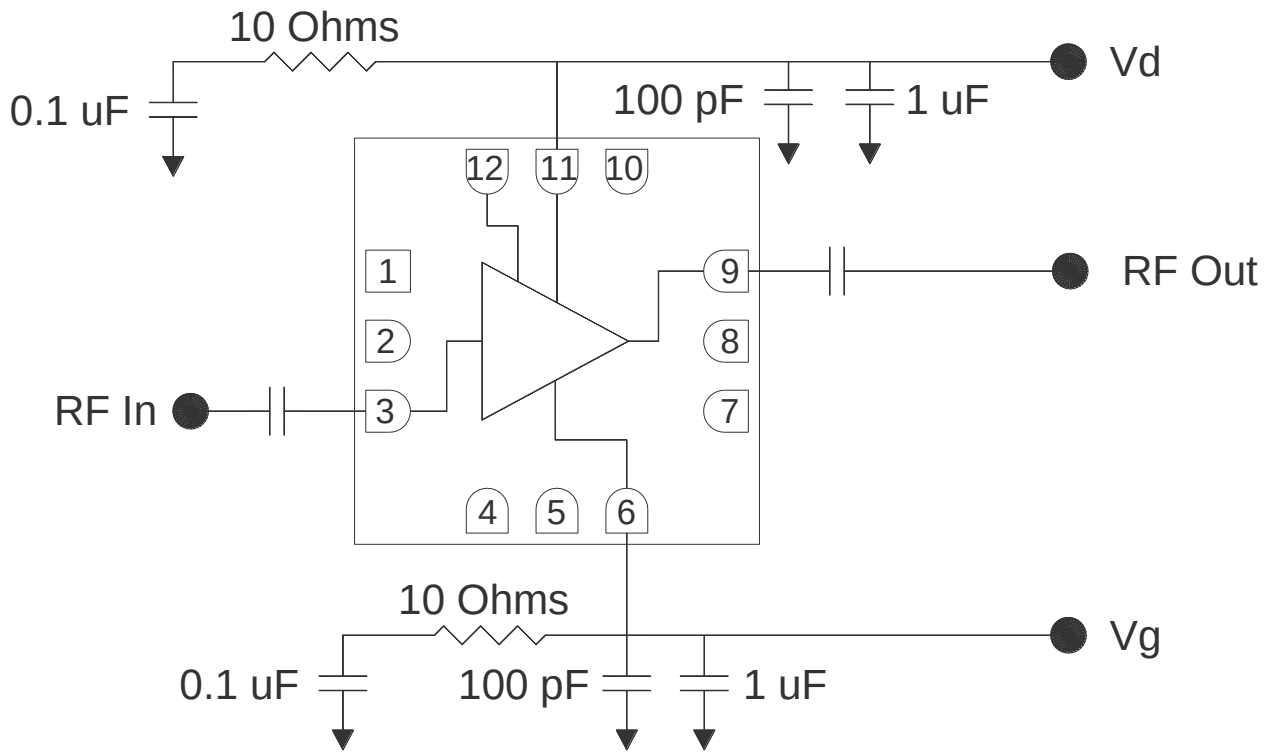








Functional Diagram and Application Circuit – Internal Positive Bias Tee (Pin 11)



Biasing and Operation

RF In / RF Out – Input and output signals should be connected by 50 ohm microstrip or coplanar traces to well matched 50 ohm sources and loads. DC blocking capacitors are required.

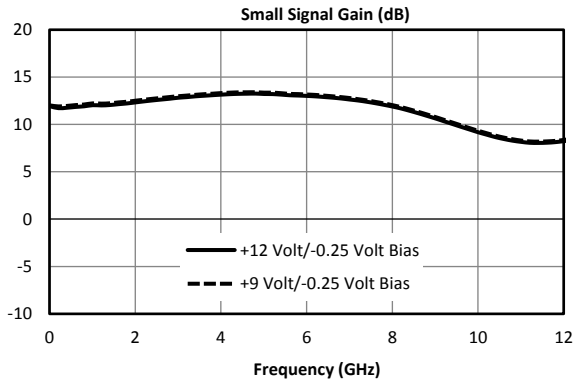
Vg – Recommended bias on this pin is -0.1 to -0.3 Volts. Harmonic generation is significantly affected by the negative gate voltage level. The amplifier is designed for optimal performance when the negative gate voltage is tuned such that the *positive* bias supply is 85 mA. It may be supplied through pin 6 or through the RF input on pin 3.

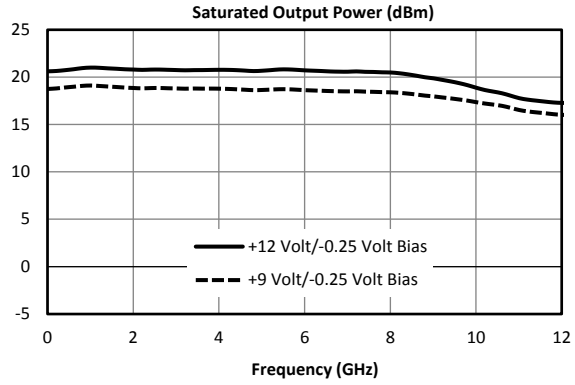
Vd- Bias supply on Vd through pin 11 should be voltage limited below 13 V and current limited below 150 mA at all times. The operational bias voltage should be between 10 V and 12 V for full gain, efficiency, and linearity. In general gain, linearity, and output power will increase marginally with increased voltage from 10 V to12 V. When the internal positive bias tee is used, pin 12 is left DC and RF open circuited and should not be connected to ground.

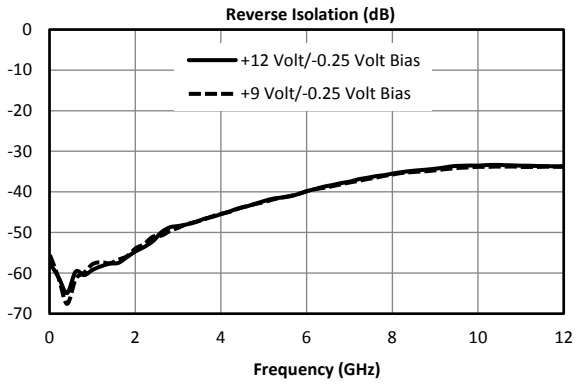
Optional Bias Circuitry – The resistor and capacitor on the Vd and Vg lines (pads 11, 12, and 6) prevent low frequency oscillation. These components are not required in bias circuits with sufficient low frequency loss. Designers should experiment to determine if they are necessary.

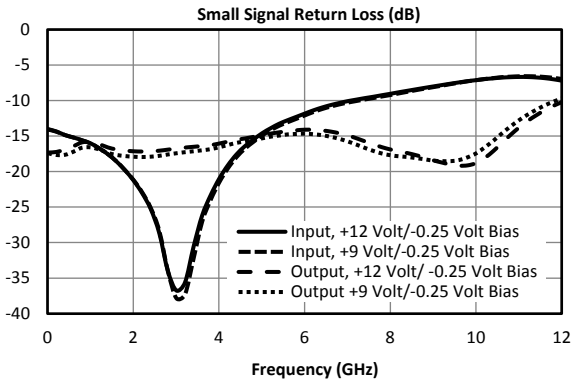
DC/RF Ground – The ground paddle of the QFN should be connected to a low noise RF and DC ground with very low electrical and thermal resistance for high frequency operation and thermal heat sinking.

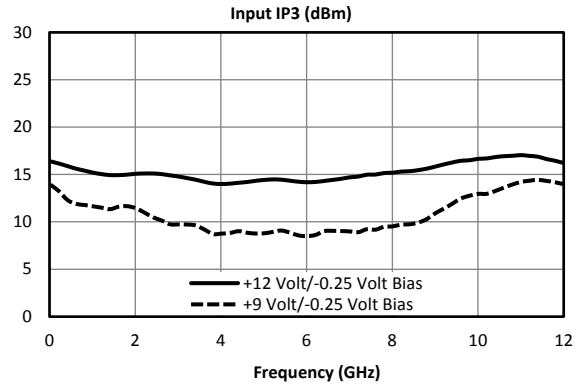
Typical Performance – +9 to +12V Internal Bias (Pin 11), -0.25 Negative Bias (Pin 6)

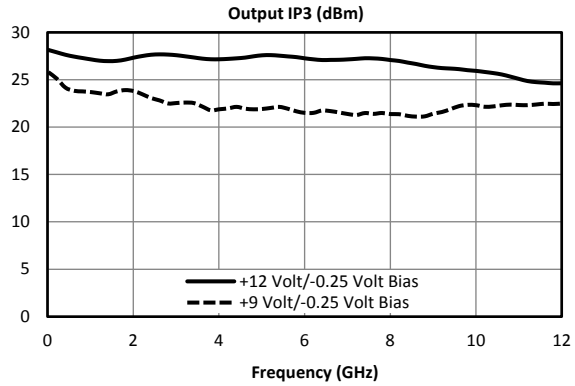




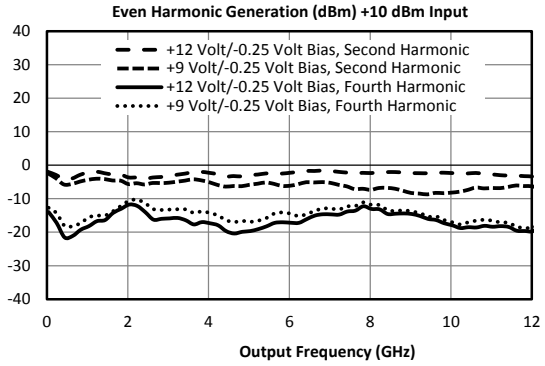


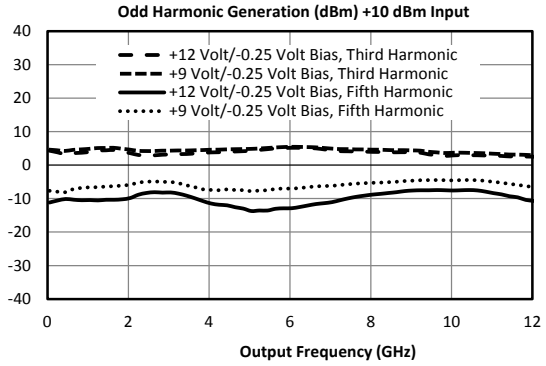


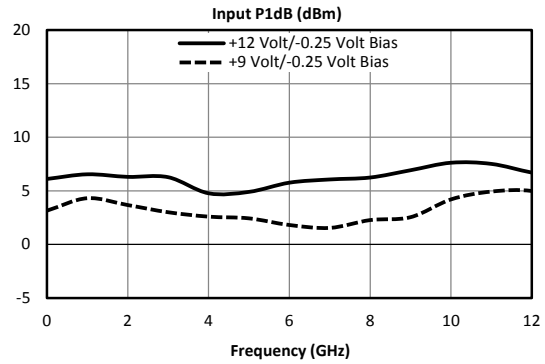


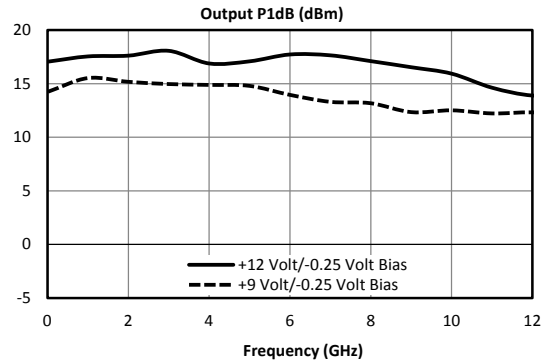


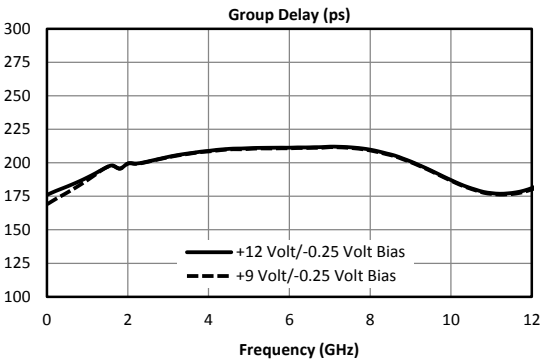
Typical Performance – +9 to +12V Internal Bias (Pin 11), -0.25 Negative Bias (Pin 6), continued

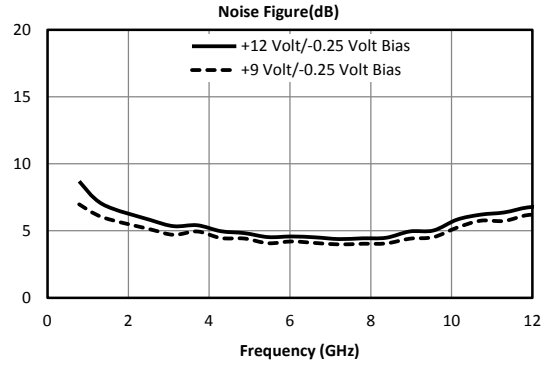


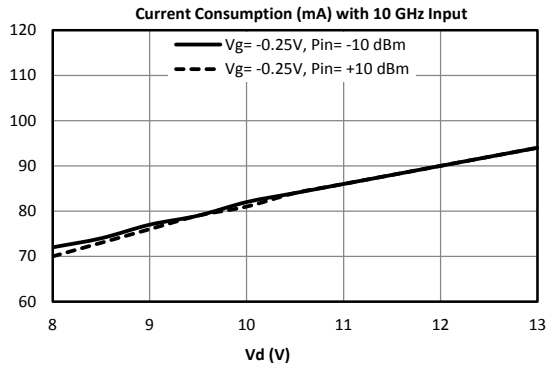




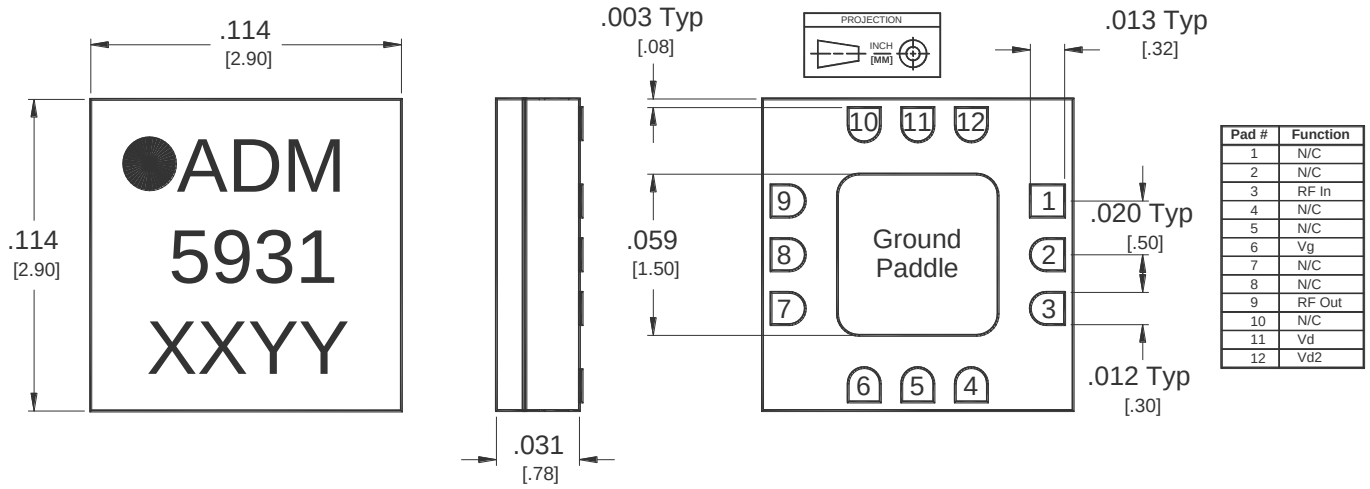








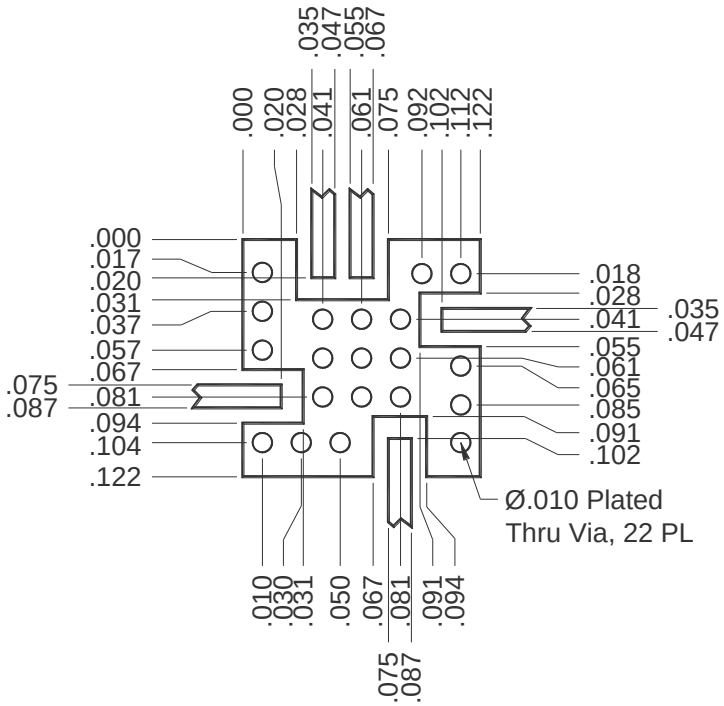
Outline Drawing



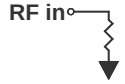
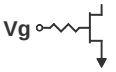
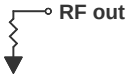
Pad #	Function
1	N/C
2	N/C
3	RF In
4	N/C
5	N/C
6	Vg
7	N/C
8	N/C
9	RF Out
10	N/C
11	Vd
12	Vd2

Substrate material is Ceramic.
I/O Leads and Ground Paddle are 1.4±0.6 microns (55±24 micro-inches) Au over 1.3 microns (51 micro-inches) Ni.
All unconnected pads should be connected to PCB RF ground.

PCB Footprint Drawing

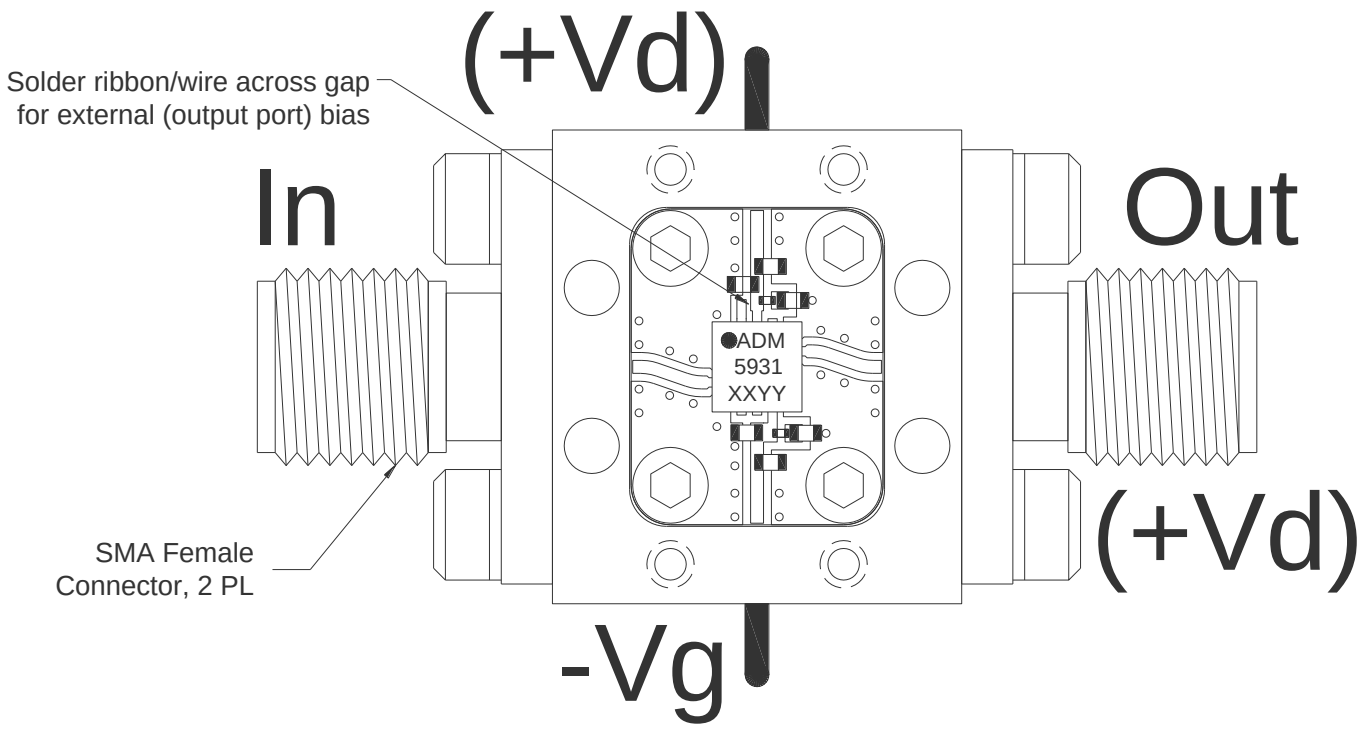


QFN-Package Surface-Mount Landing Pattern
Click here for a DXF of the above layout.
Click here for leaded solder reflow. Click here for lead-free solder reflow.

Pin Descriptions			
Pin Number	**Function**	**Description**	**Interface Schematic**
1, 2, 4, 5, 7, 8,10	NC	These pins are not connected internally. Datasheet performance is tested with NC pins grounded.	
3	RF in	This pin is DC coupled and matched to 50 Ω.	
6	Vg	Gate control for the amplifier. External decoupling resistor/capacitor is required.	
9	RF out	This pad is DC coupled and matched to 50 Ω.	
11	Vd	Power supply voltage for the amplifier. External decoupling resistor/capacitor is required.	
12	Vd2	This pin is left open for Internal Vd Bias. This pin is connected to Pin 11 (Vd) for external bias (pin 16 with bias tee).	
Paddle	GND	Ground pad should be connected to RF/DC ground with low electrical and thermal resistance.	

Absolute Maximum Ratings	
Parameter	**Maximum Rating**
Positive Bias Voltage – External Bias Tee	9 V
Positive Bias Bias Voltage – Internal Bias Tee	13 V
Positive Bias Current	150 mA
Negative Bias Voltage	-2 V
Negative Bias Current	2 mA
RF Input Power	+15 dBm
Power Dissipation	875 mW
Thermal Resistance, θ_{jc}	1.469 C/W
ESD (Human Body Model)	Class 0
Operating Temperature	-55ºC to +85ºC
Storage Temperature	-65ºC to +150ºC

Evaluation Board



The evaluation module follows Marki standard assembly and evaluation procedures to give optimal performance for datasheet characterization. Actual QFN performance will depend on substrate material, bypass capacitors, resistors, connectors, quality of bias current/voltage source, and assembly process.

Evaluation Board Bill of Materials	
Item	**Description/Part Number**
Connectors	Southwest 214-510SF
Bias Pins	Kovar
Housing	Aluminum
Circuit	.008 Thick Rogers 4003
1 uF Capacitor	TDK C1005X5R1V105K050BC
100 pF Capacitor	KEMET C0402C101K4GACTU
0.1 uF Capacitor	AVX 0402YD104KAT2A
10 Ω Resistor	Venkel CR0201-20W-100JT
ADM 5931	ADM-0012-5931SM

DATA SHEET NOTES:

1. Specifications are subject to change without notice. Contact Marki Microwave for the most recent specifications and data sheets.