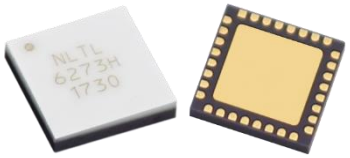
1. Device Overview

1.1 General Description

NLTL-6273SM is a MMIC non-linear transmission line (NLTL) based comb generator. This NLTL offers excellent phase noise performance over a low 0.7 to 5 GHz input frequency range with output tones to 24 GHz. NLTL-6273SM is fabricated with GaAs Schottky diode based varactors and packaged into a surface mount 5x5 mm^2 QFN.



QFN

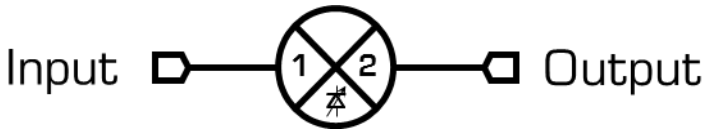
1.2 Features

- Low Phase Noise
- Broadband Input Frequencies
- No External DC Bias Required

1.3 Applications

- Comb Line Generation
- High Efficiency Multiplication
- Samplers
- Phase Locked Loops

1.4 Functional Block Diagram



1.5 Part Ordering Options[1]

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
NLTL-6273SM	5mm QFN	SM	**RoHS**	Active	EAR99
EVAL-NLTL-6273	Connectorized module, QFN reflowed onto PCB	EVAL		Active	EAR99

[1] Refer to our website for a list of definitions for terminology presented in this table.

Table of Contents

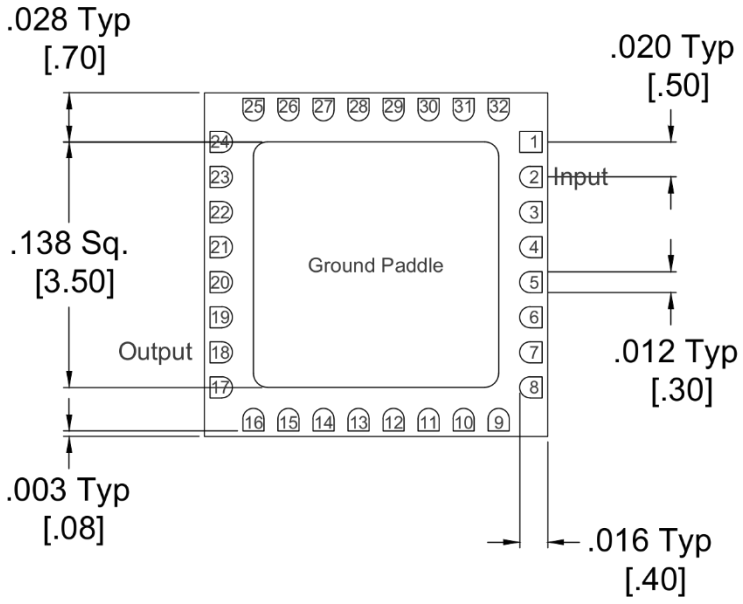
Revision History

Revision Code	Revision Date	Comment
-	October 2017	Datasheet Initial Release

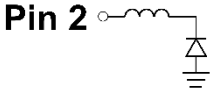
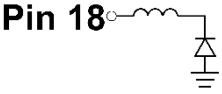
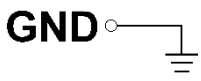
2. Port Configurations and Functions

2.1 Port Diagram

A bottom-up view of the NLTL-6273's SM package outline drawing is shown below. The NLTL should only be used in the forward direction, with the input and output ports given in Port Functions.



2.2 Port Functions

Port	Function	Description	Equivalent Circuit for Chip
Pin 2	Input	Pin 2 is DC open for the SM package.	
Pin 18	Output	Pin 18 is DC open for the SM package.	
GND	Ground	SM package ground path is provided through the ground paddle.	

3. Specifications

3.1 Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may be inoperable or have a reduced lifetime.

Parameter	Maximum Rating	Units
Port 1 DC Current	TBD	mA
Port 2 DC Current	TBD	mA
Power Handling, at any Port	+TBD	dBm
Operating Temperature	-55 to +100	°C
Storage Temperature	-65 to +125	°C

3.2 Package Information

Parameter	Details	Rating
ESD	Human Body Model (HBM), per MIL-STD-750, Method 1020	TBD
Weight	S Package	10 g

3.3 Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the electrical specifications. For limits, above which damage may occur, see Absolute Maximum Ratings.

	Min	Nominal	Max	Units
T_A, Ambient Temperature	-55	+25	+100	°C
Input Power	+16		+26	dBm

3.4 Sequencing Requirements

This is a passive NLTL that requires no external DC bias. Self-bias of the diodes is sufficient for operation. It is not required, but is recommended to provide a 50Ω termination to each port before applying RF power.

3.5 Electrical Specifications

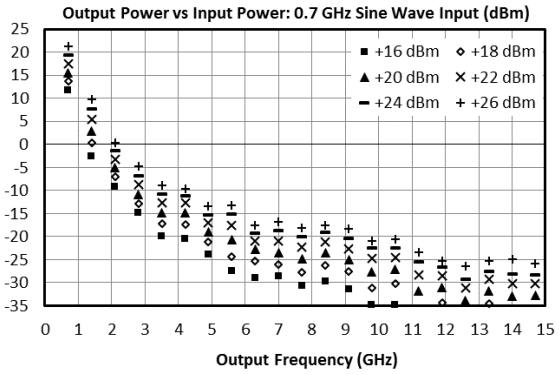
The electrical specifications apply at T_A=+25°C in a 50Ω system. Typical data shown is for the NLTL used in the forward direction with a +20 dBm sine wave[2] input.

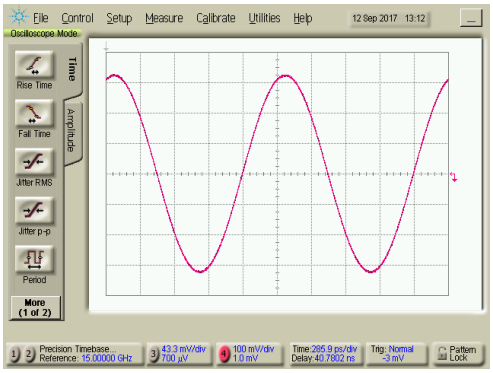
Min and Max limits apply only to our connectorized units and are guaranteed at T_A=+25°C. All bare die are 100% DC tested and visually inspected.

Parameter	Test Conditions	Min	Typical	Max	Units
Input (Port 1) Frequency Range		0.7		5	GHz
Output (Port 2) Frequency Range		0.7		24	
Input Power		+16		+26	dBm
Maximum Output Harmonic for given Input	700 MHz Input			8	-
	1 GHz Input			24	
	2 GHz Input			12	
	4 GHz Input			8	
	5 GHz Input			6	

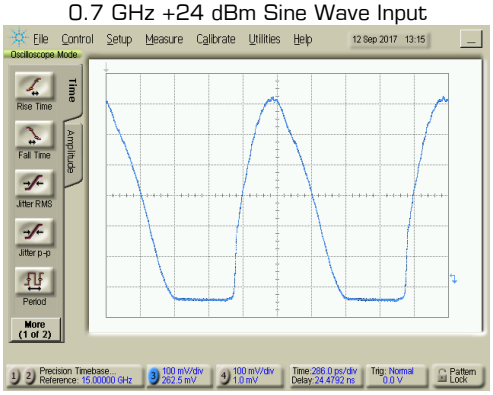
[2] Square Wave input generated using the ADM1-0026-5931SM and ADM1-0026-5929SM amplifier chain at +7 V_d/-0.5 V_g with a +12 dBm input into the amplifier.

3.6 Typical Performance Plots





0.7 GHz +24 dBm Sine Wave Input



NTL Output for 0.7 GHz +24 dBm Sine Wave Input

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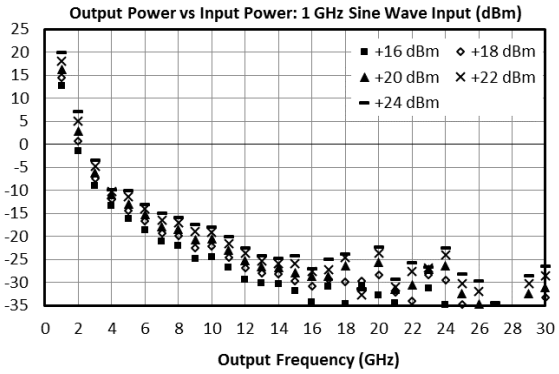
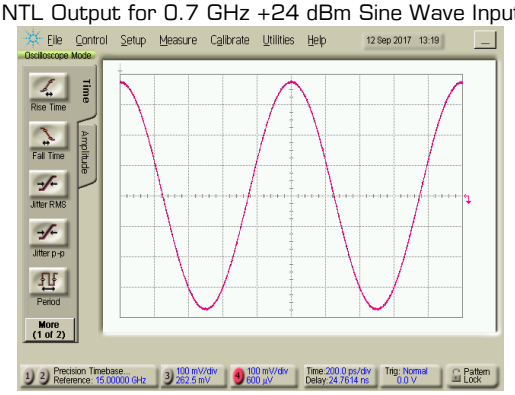
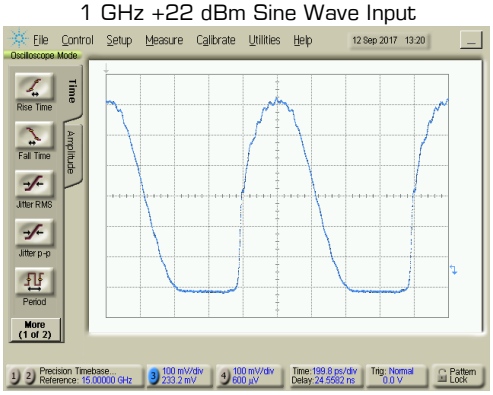




1 GHz +22 dBm Sine Wave Input



NLTL Output for 1GHz +22 dBm Sine Wave Input

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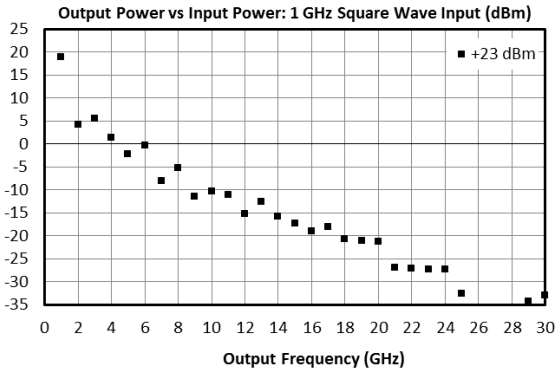
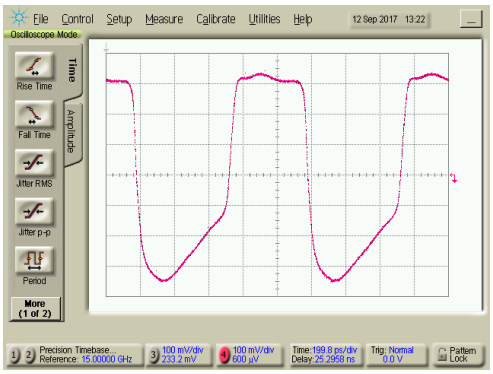
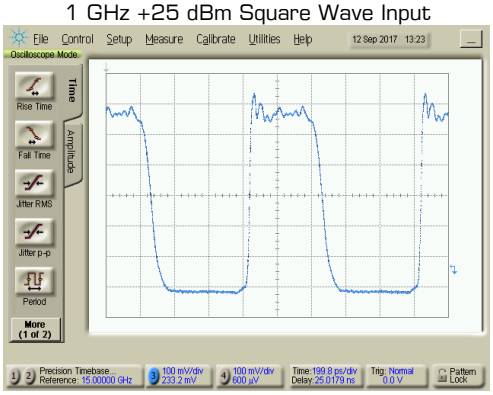




1 GHz +25 dBm Square Wave Input



NLTL Output for 1GHz +25 dBm Square Wave Input

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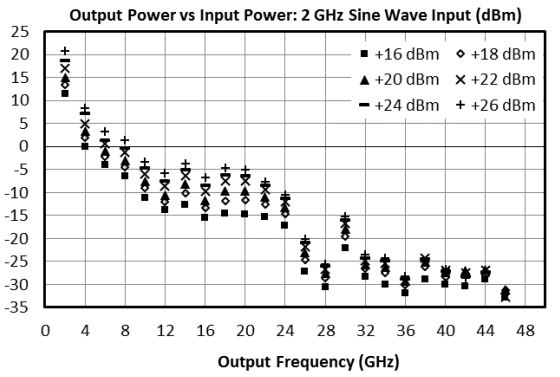
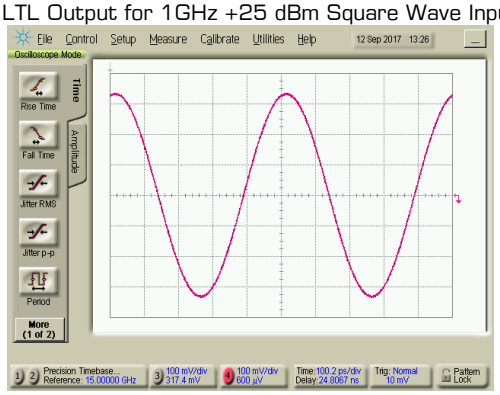
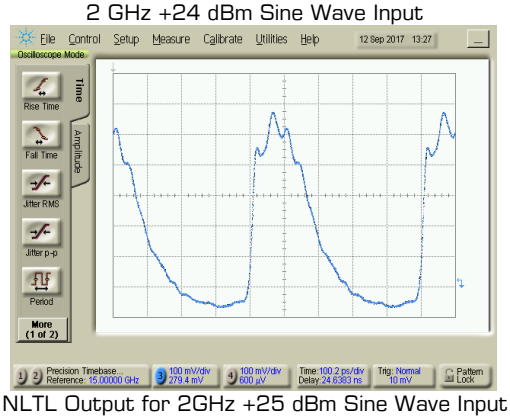




2 GHz +24 dBm Sine Wave Input



NLTL Output for 2GHz +25 dBm Sine Wave Input

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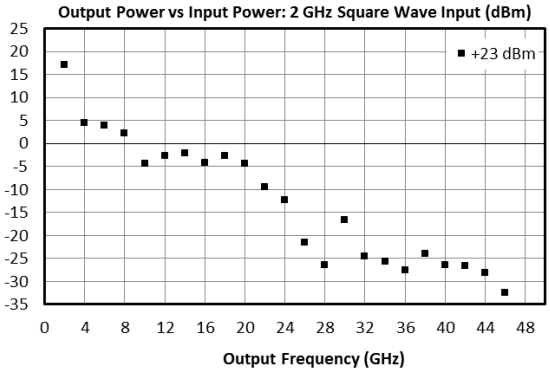

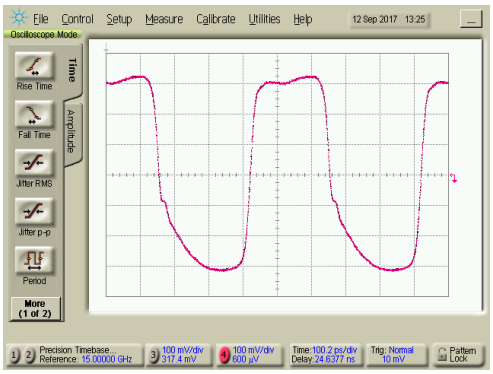

2 GHz +25 dBm Square Wave Input

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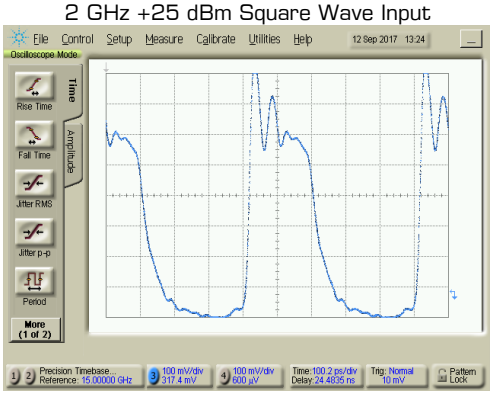
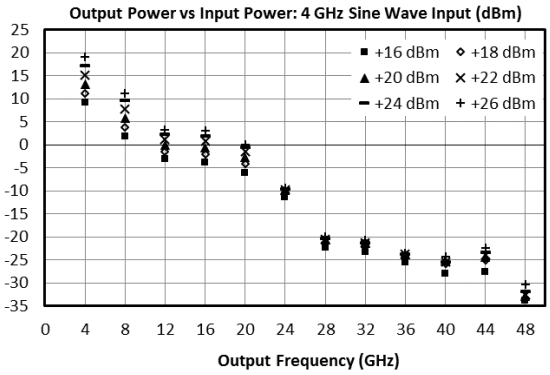
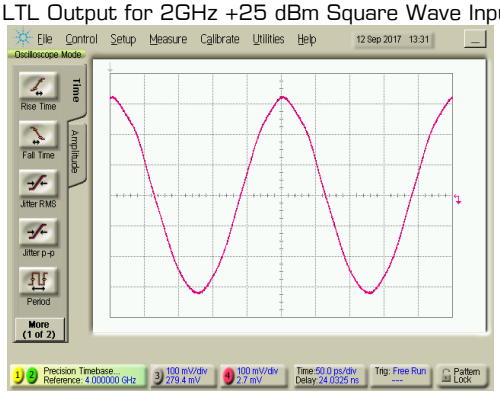


NLTL Output for 2GHz +25 dBm Square Wave Input





4 GHz +24 dBm Sine Wave Input

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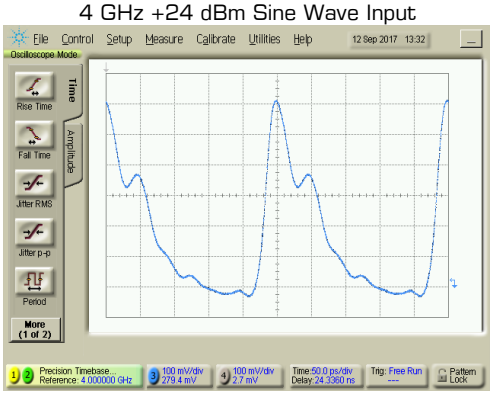
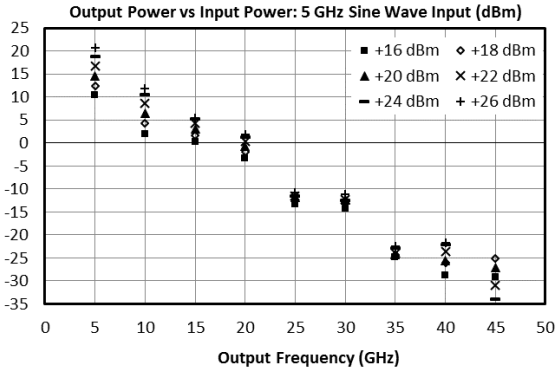
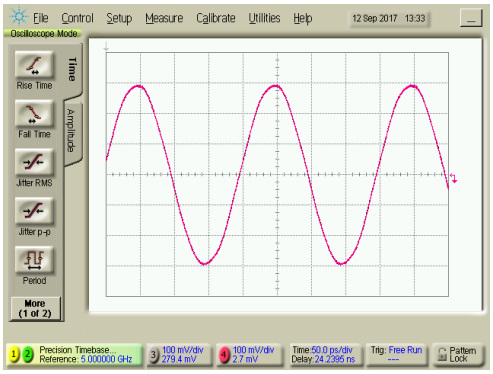


NLTL Output for 4GHz +24 dBm Sine Wave Input





5 GHz +24 dBm Sine Wave Input

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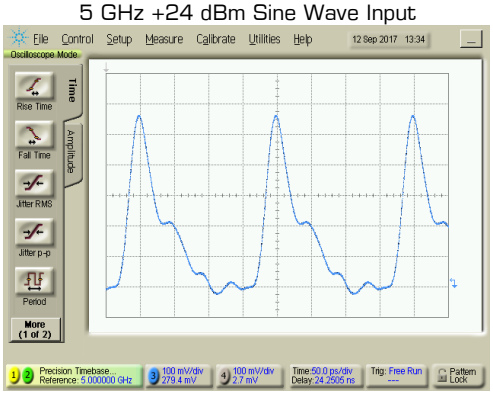
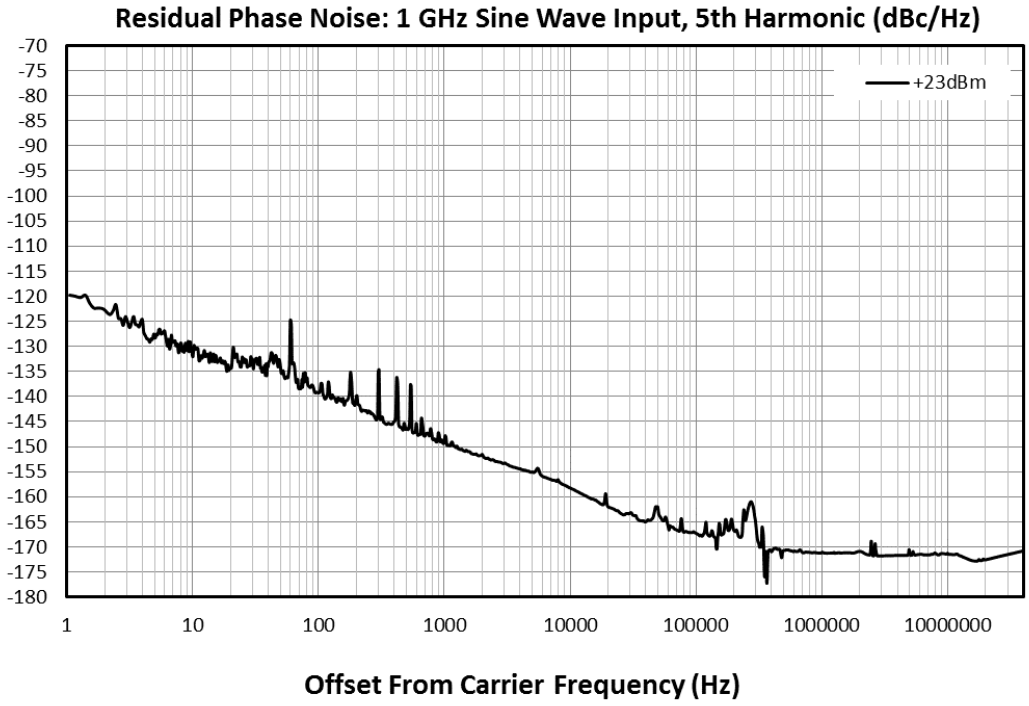


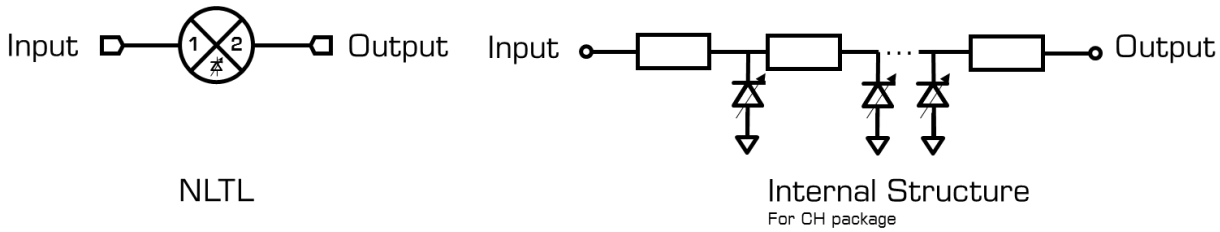
NLTL Output for 5GHz +24 dBm Sine Wave Input

3.6.1 Typical Performance Plots: Residual Phase Noise



1 GHz, +23 dBm Sine Wave Input	Parameter	Min	Typical	Max	Units
5th Output Harmonic	1 Hz Offset		-120		dBc/Hz
	10 Hz Offset		-130		
	100 Hz Offset		-140		
	1 KHz Offset		-150		
	10 KHz Offset		-160		
	100 KHz Offset		-170		
	1 MHz Offset		Thermal Floor		

4. Application Information



4.1 Detailed Description

NLTL-6273SM belongs to Marki Microwave's NLTL family of multipliers and non-linear transmission lines. The NLTL product line consists of passive GaAs MMIC non-linear transmission lines designed and fabricated with GaAs Schottky diode based varactors. NLTLs take an input signal and create an impulse train of harmonics. Harmonic outputs up to and beyond 24 GHz are generated by the NLTL. The NLTL-6273SM is the packaged 5 mm QFN version of the NLTL-6273CH.

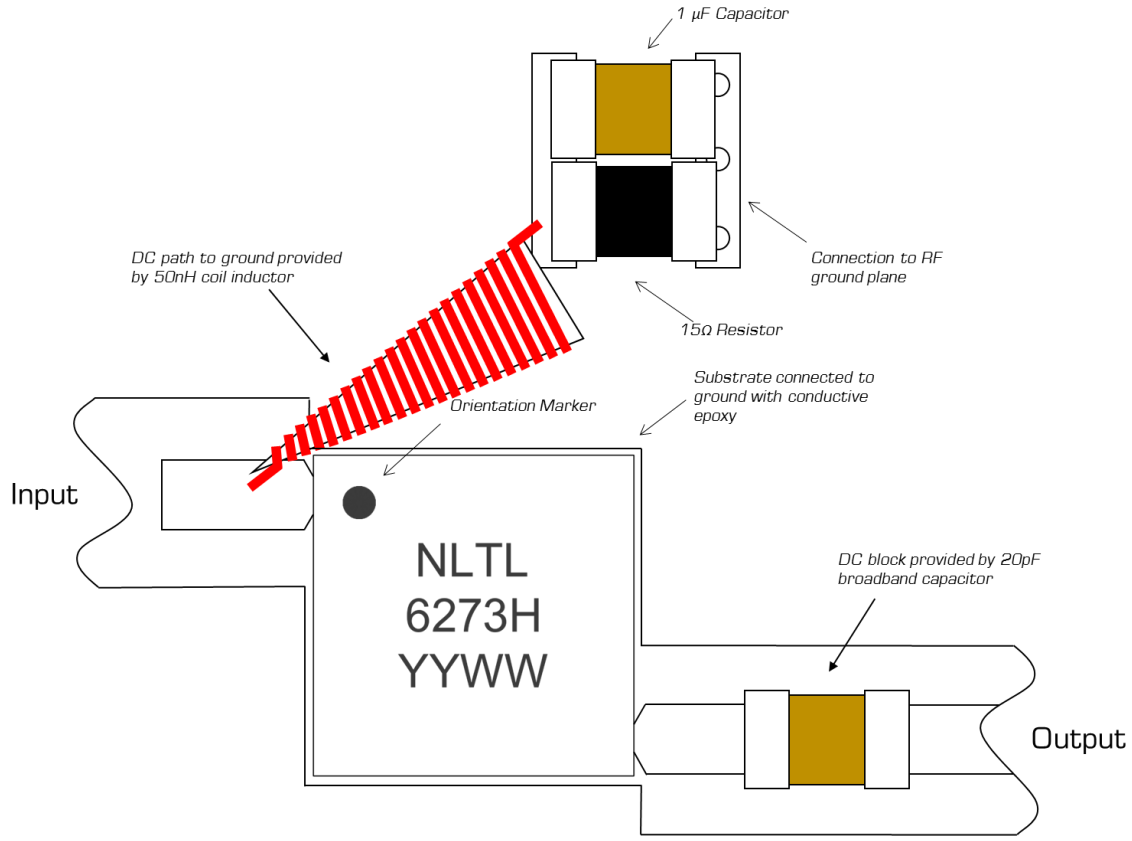
Port 1 supports L and S band input signals. Port 2 will output integer multiples of the input signal (i.e., x2, x3, x4, …, x24) up to the 24th output harmonic or a maximum of 24 GHz. Higher harmonics can be generated but will be at a lower efficiency.

The operating conditions of the NLTL are extremely important to optimize performance. High power inputs will increase the output power observed; however, the conversion efficiency will decrease. This is increasingly true for higher input frequencies and at input powers above the recommended limit. Optimal conversion efficiency of the NLTL is achieved using a square wave input with a fast rise time. Doing so causes a degradation in the 2nd output harmonic but otherwise improves the conversion efficiency at all other harmonics.

NLTL-6273SM requires no external DC bias. The self-bias of the diodes caused by the rectified RF input signal is sufficient for operation. For the best performance, optimization of the DC return path is recommended for each specific application to optimize the harmonic output power distribution.

The phase noise of a non-linear transmission line is outstanding. If verification of performance is necessary, the application circuit used and input conditions are extremely important. NLTLs are AM sensitive. If there is excessive AM noise on the input of the NLTL, observing the output of the NLTL will show excessive PM/phase noise because of the high AM to PM conversion property of NLTLs.

4.2 Application Circuit

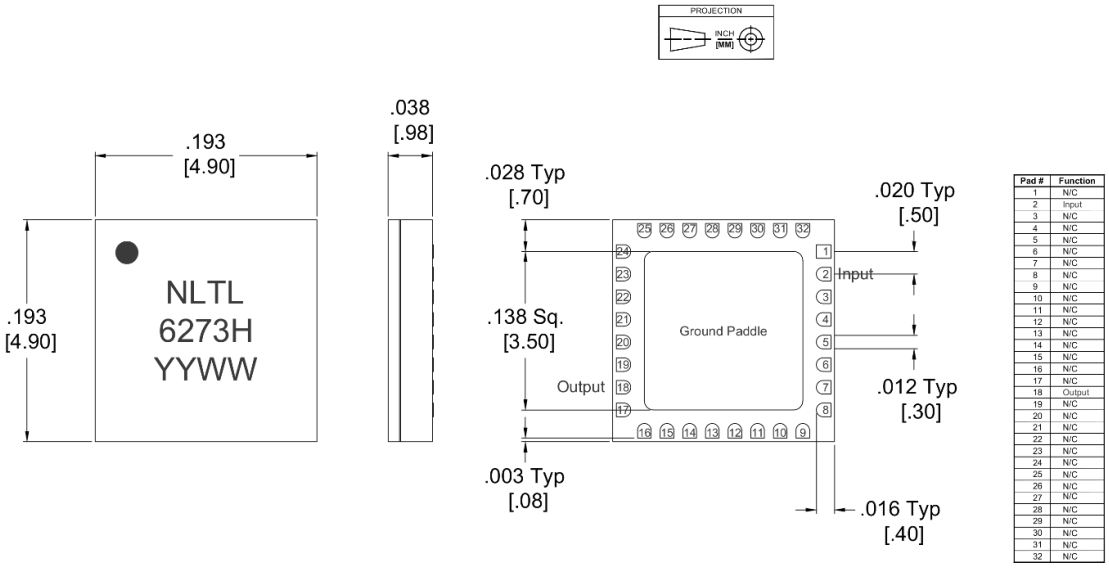


DC Path to Ground — An RF choke followed by a 15 Ω resistor should be used to provide a DC path to ground on the input port of the NLTL. A shunt 1 µF capacitor is used to filter noise generated by the resistor. This forms the circuit which self-biases the NLTL. The DC return to ground removes DC rectified current created by high power RF signal injection. The DC path to ground is provided within the S package. A conical coil inductor is recommended to push the self-resonance frequency of the inductor past the operating bandwidth of the NLTL. The recommended inductance value of the conical coil inductor is 50nH or higher.

Blocking Capacitor — A DC blocking capacitor on the output of the NLTL-6273SM's integrated circuit is necessary to prevent unwanted DC current flow from or to the output. If there is a DC signal on the input, place a DC block on the input to avoid disrupting the self-biasing of the diodes.

5. Mechanical Data

5.1 SM Package Outline Drawing



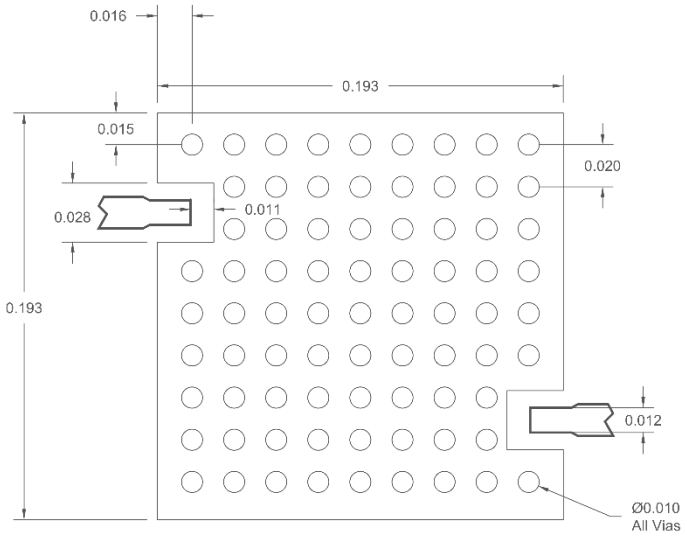
Pad #	Function
1	N/C
2	Input
3	N/C
4	N/C
5	N/C
6	N/C
7	N/C
8	N/C
9	N/C
10	N/C
11	N/C
12	N/C
13	N/C
14	N/C
15	N/C
16	N/C
17	N/C
18	Output
19	N/C
20	N/C
21	N/C
22	N/C
23	N/C
24	N/C
25	N/C
26	N/C
27	N/C
28	N/C
29	N/C
30	N/C
31	N/C
32	N/C

1. Substrate material is ceramic.
2. I/O Leads and Ground Paddle plating is (from base to finish):

Ni:	8.89um MAX	1.27um MIN
Pd:	0.17um MAX	0.07um MIN
Au	0.254um MAX	0.03um MIN

3. All unconnected pads should be connected to PCB RF ground.

5.2 SM Package Footprint



QFN-Package Surface-Mount Landing Pattern
Click here for a DXF of the above layout.
Click here for leaded solder reflow. Click here for lead-free solder reflow

5.3 Evaluation Board Outline Drawing